RFSoC-based high-speed Digitizer with 8 Channels, 5.0 GSPS / 14 Bits

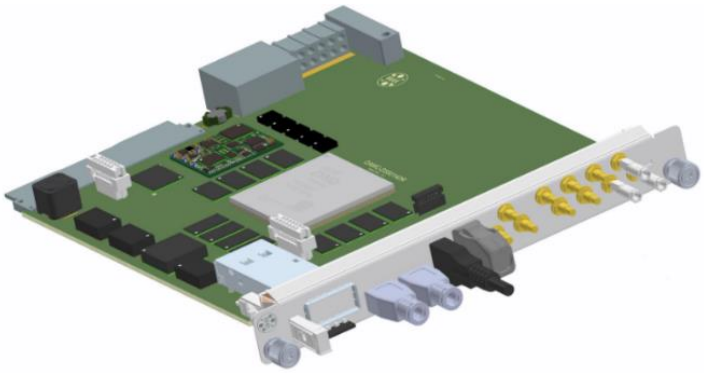
DAMC-DS5014DR

HIGHLIGHTS

- 6.0 GHz analog bandwidth (-3 dB)
- Single-ended analog RTM connection (Class RF1.1)
- 8 analog inputs and 8 analog outputs via RTM
- Alternatively up to 8 analog inputs and/or outputs on front panel via coaxial SSMC connector
- 5.0 GSPS per channels ADC sampling rate
- 3x DDR4 banks with up to 48 GB DRAM
- Dual-Loop Low-Jitter PLL On-Board
- 9.85 GSPS per channels DAC data rate
- Up to 12 Trigger inputs and one Trigger output

FEATURES

- FPGA: AMD Ultrascale+ RFSoC XCZU47DR
- Analog signal range 1 Vpp
- AC or DC coupling, depending upon assembly variant
- Internal or external clock reference and ref. output
- White Rabbit support
- Event timestamp
- 8 Gsamples+ data memory (ADC: 14 bits, Timestamp: 32 bits)
- PCIe Gen.4 x 8 and 100G Ethernet data interfaces
- Fully customized firmware code available for fast data processing
- FPGA open for custom application (open-source BSP)
- Yocto Linux support
- Standalone mode (can run without AMC CPU module)
- Supported by all AMD development tools



DAMC-DS5014DR

The DAMC-DS5014DR is the most versatile 14-bit, 8-channel Digitizer among the other available MTCA digitizer families. It offers a broad range of sample rates at the MicroTCA form factor and a selectable AC or DC-coupled analog front-end, making it ideal for various detectors in advanced measurement scenarios. Its exceptional dynamic performance makes the DS5014DR well-suited for pulse-capture applications and RF/IF sampling.

Building Block

The core component of the DS5014DR module is the AMD Zynq UltraScale+ RFSoC. The chip offers low-noise ADCs with a sampling rate up to maximum 5 GSPS with a wide input bandwidth of 6 GHz and low-noise DACs with a high sampling rate of 9.85 GSPS, which are attractive components for a multiple of scientific applications.

The RFSoC includes plenty of digital resources and multi-core ARM processors that are combined with 3 independent DRAM channels for versatile processing implementations.

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Analog Front-end

In the DS5014DR, a range of assembly options is provided to enable scientists to utilize the entire ADC/DAC bandwidth, including DC or AC coupling. For applications such as detector pulse processing where the signal has a DC component, DC coupling is essential. Moreover, the user's ability to adjust the DC level of the pulses empowers them to fully utilize the dynamic range of the ADC. For those applications where the input signals are continuous waveforms (CW) and need direct sampling and processing of the RF/IF signals, it is recommended that AC coupling is used.

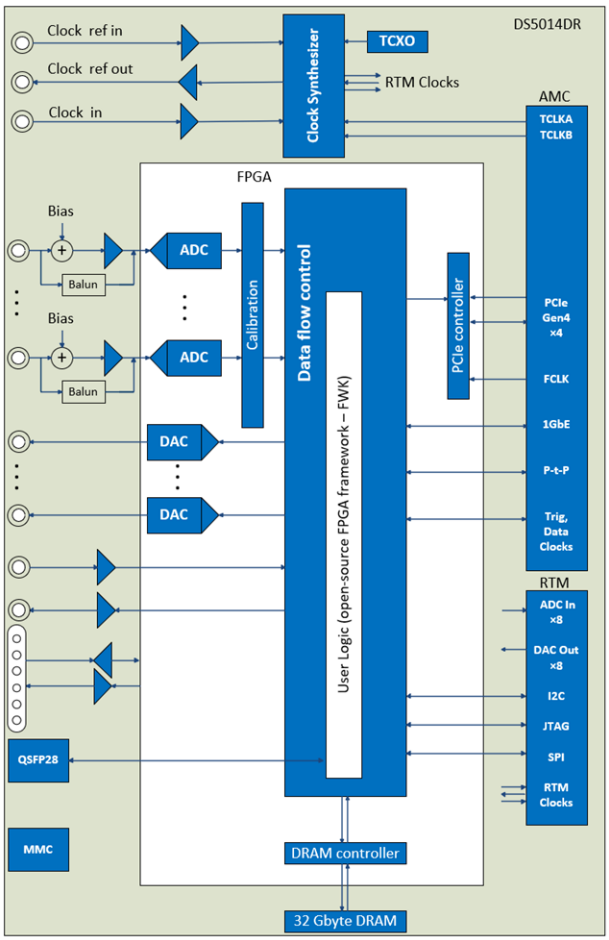

Figure 1: Block Diagram of the DAMC-DS5014DR.

Open-Source Firmware development framework (FWK)

To facilitate application development and signal processing with the DS5014DR board, DESY offers open-source FPGA example firmware and a board-support package (BSP). This structure allows the application developers to focus on the higher-level application layer, where they can integrate their algorithms and access high-speed ADC/DAC data.

Moreover, an embedded Linux image was generated using Yocto, which is fully supported by the provided firmware. The firmware is built using DESY's open-source FPGA framework, FWK, which is actively maintained by the MSK group at DESY.

Storage Memory

The DS5014DR includes a few different high-density memories connected to the RFSoC.

The fast data recording and processing memory includes three separate DDR4 DRAM channels, each with 64 bits and up to 16 GByte each at a data transfer rate of up to 2666 MT/s. The AMC PCIe interface to the host PC enables up to 15.7 GBytes/s payload data transfer over a PCIe Gen.4 interface with up to eight transmission lanes. Alternatively, the data can be transferred via 100 Gigabit Ethernet on the front panel.

Additionally, DS5014DR contains other nonvolatile memories to store the firmware, configuration data, calibration parameters and the image of the Embedded Linux kernel.

High-Speed Digitizer DAMC-DS5014DR

TECHNICAL SPECIFICATIONS

ARCHITECTURE			
Physical Dimensions		Double width, Mid-Size with Full-Size option Width: 5.486” (148.5 mm) Depth: 7.110” (180.6 mm)	
Standards		MTCA.4	Advanced Mezzanine Card
		Module management	DMMC-STAMP (IPMI Version 2.0)
Compatibility		Zone 3 classification	Class RF1.1
		Compatible RTM products	
Type electrical properties		FPGA Type	AMD Ultrascale+ RFSoC XCZU47DR-1FFVG1517E
		FPGA Resources	930k Logic Cells / 24x GTY (28.21GBPS) / 4272 DSP slices
		Power consumption	<50 W, depending on FPGA bitstream
		Typical latency	< 100 ns
Components	RAM	2x DDR4-2666 + 1x DDR4-2400 SDRAM	64bis each, up to 48 GByte
	PROM	QSPI FLASH / eMMC / SD card	redundant 1 Gbit NOR FLASH / 16 GB industrial eMMC / MicroSD
	ADC	Sampling Rate	Up to 5 GSPS @ 14 bits resolution
		Analog Bandwidth	6 GHz FPBW (-3dB)
		Analog Front End	AC or DC coupling up to 6.0 GHz
	DAC	Sampling Rate	Up to 9.85 GSPS @ 14 bits resolution
		Analog Bandwidth	6 GHz FPBW (-3dB)
		Analog Front End	AC coupling up to 6.0 GHz
	PLL	Reference Clock Input	up to 4 GHz
		Clock output	2x to the Front Panel or to the RTM
Front panel	Digital IOs	QFP28 Module	4 x 28.0 Gbps data throughput, compatible to 100GE for PCIe
		Mirco USB-B	Command-line debug Interface
		USB-C	USB Host (Linux) and Display-Port with boot media support
		Trigger Inputs	4
	Analog	Front panel	8 channels
		Connector type	SSMC
		Matching	50 Ω AC/DC
		Maximum input power level	
Backplane	Low latency connection	Point-to-Point (LLL) Connection	4 channels
		Interface type	Peer-to-peer, ports 8-15 according to AMC specification
		Data throughput	12.5 Gbps per lane
		Bit error rate	$<10^{-12}$ bit^{-1}
	PCIe	Backplane	8 or 4 lanes
		Interface type	PCIe Gen. 4.0 (128 GSPS Throughput using x8 link on backplanes with x8 topology)

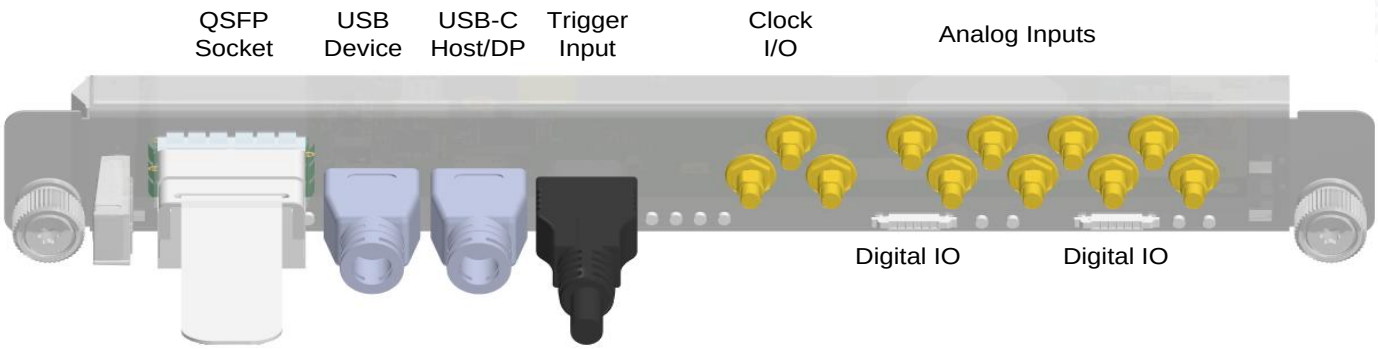

Figure 2: DAMC-DS5014DR Front Panel.

High-Speed Digitizer DAMC-DS5014DR

TECHNICAL SPECIFICATIONS

Key Parameters	
ADC Resolution	14 bits
Analog input Channels	8
Signal range	1 Vpp
Bias settings*	Full signal range
Bias setting steps*	4096 levels
Sample rate per channel	Up to 5 GSPS
Impedance DC/AC	50 Ω
Over voltage protection	5 Vpp
Analog Bandwidth	DC Mode: DC – 6.0 GHz AC Mode: 0.03 – 6.0 GHz

* - Bias level only available on the DC coupling mode.

DAC	
DAC Resolution	14 bits
Analog output Channels	8
Signal range setting	0.64 Vpp to 3.2 Vpp -21.5 dBm to 3.0 dBm
Range setting steps	1024
Sample rate per channel	Up to 9.85 GSPS
Impedance AC	50 Ω
Analog Bandwidth	AC mode: 0.03 – 6.0 GHz DC Mode: DC – 2.5 GHz

AC data 32 MHz 8 CH 240 MSPS					
Range	SNR	SINAD	THD	SFDR	ENOB
1 Vpp	-	-	-	84	-

- To be updated.

AC data 32 MHz 8 CH 2.4 GSPS					
Range	SNR	SINAD	THD	SFDR	ENOB
-	-	-	-	-	-

- To be updated.

AC data 32 MHz 8 CH 5.0 GSPS					
Range	SNR	SINAD	THD	SFDR	ENOB
-	-	-	-	-	-

- To be updated.

Bias Setting		
Range	MIN	MAX
1 Vpp	-0.5	0.5

GPIO		
Number of GPIOs	8	
Output impedance	33	Ω
Output (low – high)	0.1 – 3.3	V
Input impedance	10	kΩ
Input (low – high)	1 – 2.3	V
Connector	2x Molex 5037630691	

External Clock Source Input		
Frequency	0.01 – 3	GHz
Signal level	1	Vpp
Impedance AC	50	Ω
Duty Cycle	50%	
Connector	SSMC (Edge mount)	

Clock Reference Input		
Internal Clock reference		
Frequency	10	MHz
Accuracy	±5±0.5/y	ppm
External clock reference		
Frequency (min – max)	100 - 4000	MHz
Signal level (min – max)	1	Vpp
Impedance AC	50	Ω
Duty Cycle	50%	
Connector	1) SSMC (Edge mount) – Front panel 2) TE 6469081-1 – RTM side	

Clock Reference Output		
Frequency	10 – 3000	MHz
Signal level	1	Vpp
Impedance AC	50	Ω
Duty Cycle	50%	
Connector	1) SSMC (Edge mount) – Front panel 2) TE 6469081-1 (RTM) – Pins (10e, 10f)	

High-Speed Digitizer DAMC-DS5014DR

TECHNICAL SPECIFICATIONS

External trigger inputs		
Trigger channels LVDS	4	
Input impedance DC	100	Ω
Input range (min – max)	0.1 to 2.4	V
Threshold rising/falling edge	500	mV
Sensitivity	200	mV
Jitter	250	ps
Resolution	1/FS	s
Connector	IX61G-A-10P(01)	

External trigger output		
Trigger channels LVDS	1	
Output impedance	100	Ω
Output (low – high)	0.1 to 2.4	V
Connector	IX61G-A-10P(01)	