Low-Latency Digitizer with 8-Channels, 800 MSPS / 12Bit

DAMC-DS812ZUP

HIGHLIGHTS

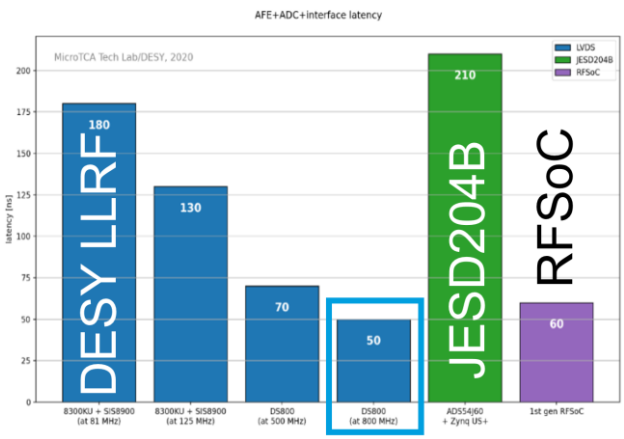
- 2.7 GHz analog bandwidth (-3dB)
- Single-ended analog RTM connection (Class RF1.0)
- Input from front (SSMC) or rear (RTM)
- 8x 800MSPS or 8x 500MSPS Variants
- Memory: 4GB DDR4-2666
- Dual-Loop Low-Jitter PLL On-Board
- 8 Trigger Inputs on Front Panel

FEATURES

- FPGA: AMD Ultrascale+ MPSoC XCZU7CG
- Dual Edge Sampling with 4x 1.6GSPS (1GSPS)
- Dual-core Cortex-A53 ARM CPU with up to 1.3GHz
- PCIe Gen.3 x 8 Interface
- QSFP+ Connector with 4x 16.3 Gbps
- 3 different sources for clocking the ADCs
- On-board dual-loop low-jitter PLL
- Ultra-stable low phase-noise OCXO clock source
- Linux Support (eMMC and MicroSD)
- Standalone mode (runs without CPU Module)
- Supported by all AMD development tools

The DAMC-DS812ZUP is an 8-channel AMC Digitizer with 800 MSPS (or 500 MSPS variants) and 12 bits resolution. In software-selectable 4-channel dual-edge sampling mode, the ADCs allow sampling at 1600 MSPS (1000 MSPS). It is the first board that implements the analog Zone 3 Class RF 1.0. The connections to the RTM are realized with single-ended coaxial connections that allow using the full 2.7 GHz analog bandwidth of the ADCs.

The ADCs are connected via parallel LVDS Interface to provide a low-latency connection. All channels can be captured simultaneously into 4GB DDR4 Memory.



Latency comparison

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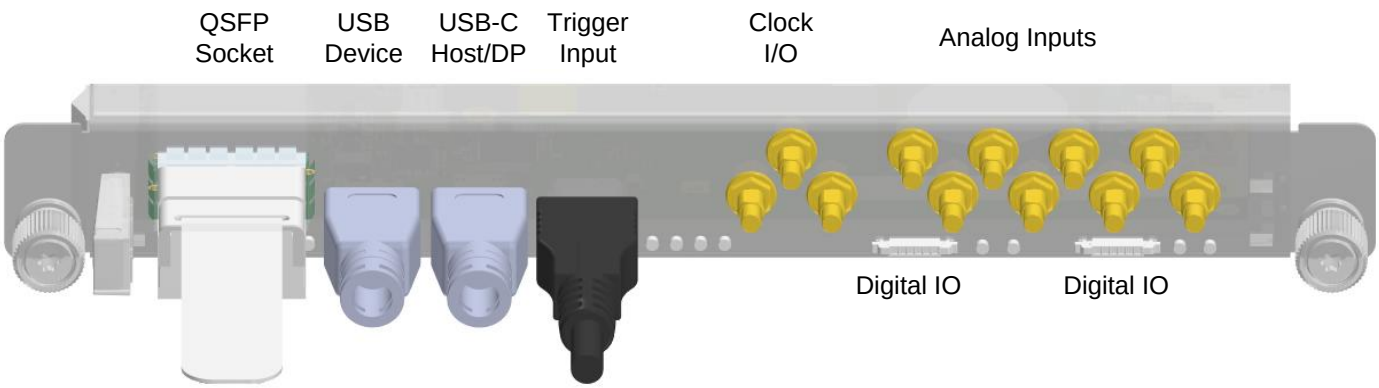
DESY

Low-Cost IO Controller Board DAMC-FMC1Z7IO

TECHNICAL SPECIFICATIONS

ARCHITECTURE

Physical Dimensions		Double width, Mid-Size with Full-Size option	
		Width: 5.486” (148.5 mm)	
		Depth: 7.110” (180.6 mm)	
Standards		MTCA.4	Advanced Mezzanine Card
		Module management	DMMC-STAMP (IPMI Version 2.0)
Compatibility		Zone 3 classification	Class RF1.0
		Compatible RTM products	
Type Electrical properties	AMC Digitizer with LVDS ADCs	Number of analog Channels	8 (4 in dual-edge Sampling mode)
		FPGA Type	AMD Ultrascale+ MPSoC XCZU7CG-1FFVF1517E
		FPGA Resources	504k Logic Cells / 24x GTH (16.3Gbps) / 1700 DSP slices
		Power consumption	<50 W
		Typical latency	
Components	RAM	DDR4-2666 SDRAM	256 M x 64 bit
	PROM	QSPI FLASH / eMMC / SD card	redundant 1 Gbit NOR FLASH / 8 GB industrial eMMC / MicroSD
	ADC	Sampling Rate	800 MSPS @ 12Bit or 500 MSPS @ 12 Bit with two ch. per ADC 1.6 GSPS @ 12Bit or 1.0 GSPS @ 12Bit Interleaved Mode
		Analog Bandwidth	2.7 GHz FPBW (-3dB)
		Analog Front End	AC or DC coupling up to 4.8 GHz
	PLL	Reference Clock Input	up to 4 GHz
		Clock output	2x to the Front Panel or to the RTM
Front panel	Digital IOs	QFP+ Module	4 x 16.3 Gbps data throughput
		Mirco USB-B	Command-line debug Interface
		USB-C	USB Host (Linux) and Display-Port (alternate mode)
		Trigger Inputs	
	Analog	Front panel	8 channels
		Connector type	SSMC
		Matching	50 Ω AC/DC
		Maximum input power level	
Backplane	Low latency connection	Point-to-Point (LLL) Connection	4 channels
		Interface type	Peer-to-peer, ports 8-15 according to AMC specification
		Data throughput	16.5 Gbps
		Bit error rate	$<10^{14}$ bit^{-1}
	PCIe	Backplane	8 or 4 lanes
		Interface type	PCIe Gen. 3.0 (64 Gbps Throughput using x8 link on backplanes with x8 topology)



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