AMC - Dual HPC-FMC Carrier

DAMC-FMC25

HIGHLIGHTS

- Dual-FPGA processing
- Two (fully populated) HPC FMC slots
- Up to 4 MGT links on one HPC slot
- Front panel clock input

FEATURES

Advanced Mezzanine Card (AMC)

- Double width, mid-size MTCA.4 form factor
- RTM Class D1.1 support
- Dual-FPGA processing
  - FPGA XC5VFX70T or XC5VFX100T for serial communication including PCIe
  - XC6SLX45T for signal processing and connectivity to RTM and FMCs
- 256 and 128 Megabytes DDR2 SD-RAM
- Rear IO connected to FPGA
- Supports 2 FMCs: 2 x HPC module
- ANSI/VITA 57.1 compliant
- Extra power connector for FMCs
- IPMI 1.1 compliant MMC
- RoHS compliant

The DAMC-FMC25 is a general purpose carrier with ability to host two FMC mezzanines high pin count (HPC) each. Virtex-5 FPGA allows to do high performance computation with high data throughput between FMCs, RTM and PCIe bus on the MicroTCA backplane. Local DDR2 memory can be used to store measurement data which couldn't be sent via PCIe during acquisition.

MicroTCA TECHNOLOGY LAB
A HELMHOLTZ INNOVATION LAB

DESY.

AMC - Dual HPC-FMC Carrier DAMC-FMC25

TECHNICAL SPECIFICATIONS

ARCHITECTURE			
Physical		Dimensions	Double-width, mid-size
			Width: 148.5mm
			Depth: 180.6mm
Standards		AMC.0, AMC.1, AMC.2, MTCA.4	Advanced Mezzanine Card (AMC)
		Module management	IPMI Version 1.5, MMC V1.0 compatible
Compatibility		Zone3 classification	Class D1.1
		Compatible RTM products	DRTM-AD84, DRTM-PZT4 etc.
		FPGA Mezzanine Card (FMC)	two high pin count (HPC) slots, ANSI/VITA 57 compliant
		Compatible FMC products	DFMC-MD22, DFMC-AD16, DFMC-SFP4, DFMC-DS800 etc.
BOARD			
Components	FPGA	Xilinx Virtex-5 and Spartan-6	XC5VFX70T (100T as a build option) and XC6SLX45T
		Speed grade	-2 for XC5VFX70T or XC5VFX100T, -3 for XC6SLX45T
		FPGA resources	Slices: 11k (16k for 100T) and 6.8k
			DSP slices: 128 (256 for 100T) and 58
	RAM	DDR2-667 SDRAM	64M x 32 bit and 64M x 16 bit
	PROM	QSPI FLASH	2 x 256 Mbit for V5, 2 x 256 Mbit for S6
	Clocks	Oscillator	200 MHz
		PLL (ICS844021BG)	125 MHz for links
		PLL (Si5338A)	programmable over I2C, 0.16 MHz to 710 MHz
		Clock inputs	External (front-panel), AMC (TCLKA, TCLKB), FMC, RTM
Electrical properties		Power consumption	Typ. < 2A for carrier + FMC mezzanines consumption
FMC SLOTS			
FMC1		LVDS differential pairs	68 (34 LA + 17 HA + 17 HB)
		Transceivers	2 (0 as a build option), 6.252 (0 as a build option), 6.2Gbps
		Other	JTAG, I2C connected to MMC
FMC2		LVDS differential pairs	68 (34 LA + 17 HA + 17 HB)
		Transceivers	2 (4 as a build option), 6.25 Gbps
		Other	JTAG, I2C connected to MMC
CONNECTIVITY			
Front panel	FMC	Front panel	2 HPC slots
	Reference clock input	Front panel	1 channel
		Connector type	SMA, single-ended
		Impedance/coupling	50 Ω/AC
		Maximum input level	2.5 Vpp
	Debug interface	Front panel	2 channel, FPGA and MMC
		Connector type	Micro USB
		Data throughput	3 Mbps
Backplane	Low latency connection	Backplane	4 channels
		Connector type	Peer-to-peer, ports 12-15 accordign to AMC specifications
		Data throughput	6.5 Gbps
		Bit error rate	$<10^{14}$ bit^{-1}
	PCIe	Backplane	4 lanes
		Connector type	PCIe Gen 1 (PCIe gen 2 possible with soft core)
		Data throughput	2.5Gbps, 5.0 Gbps
		Bit error rate	$<10^{14}$ bit^{-1}
	Gigabit Ethernet	Backplane	2 channels
		Physical layer	1000BASE-X
		Data throughput	1 Gbps
		Bit error rate	$<10^{14}$ bit^{-1}

DESY
Deutsches Elektronen-Synchrotron
Notkestr. 85 • 22607 Hamburg
mtca-techlab@desy.de
techlab.desy.de

MicroTCA TECHNOLOGY LAB

DESY.

AMC - Dual HPC-FMC Carrier DAMC-FMC25

TECHNICAL SPECIFICATIONS

CONNECTIVITY (CONTINUED)

Zone 3	Low latency connection	RTM	2 channels
		Connector type	Peer-to-peer, according to D1.1 class
		Data throughput	6.25 Gbps
		Bit error rate	$<10^{14}$ bit^{-1}
	Parallel bus	RTM	42 differential pairs
		Connector type	LVDS
		Data throughput	52.5 Gbps
		Bit error rate	$<10^{14}$ bit^{-1}
	AMC clock	Clock output	2 reference clock signals
		Connector type	LVDS
		Clock frequency	50 - 325 MHz / TCLKA
	RTM clock	Clock input	1 reference clock inputs
		Clock type	FPGA global clock, GTX reference clock, PLL
	Others	MTCA.4 signals	IPMI bus - I²C, presence, power supply
		Interlocks	3 differential dedicated output signals
		JTAG	JTAG chain, +3V3

OTHER FEATURES

		RTM management	With power supply and curent monitoring
		Firmware upgrade	Yes, via IPMI and PCIe interface
		Voltage and current monitor	Yes, readout via IPMI
		LEDs	IPMI management control
		Mechanical	Hot swap ejector handle
Environmental		Operating temperature	0 … 50 °C
		Storage temperature	-40 … +90 °C
		Relative humidity	5% … 90%, non-condensing
		Weight	0.5 kg

OTHER

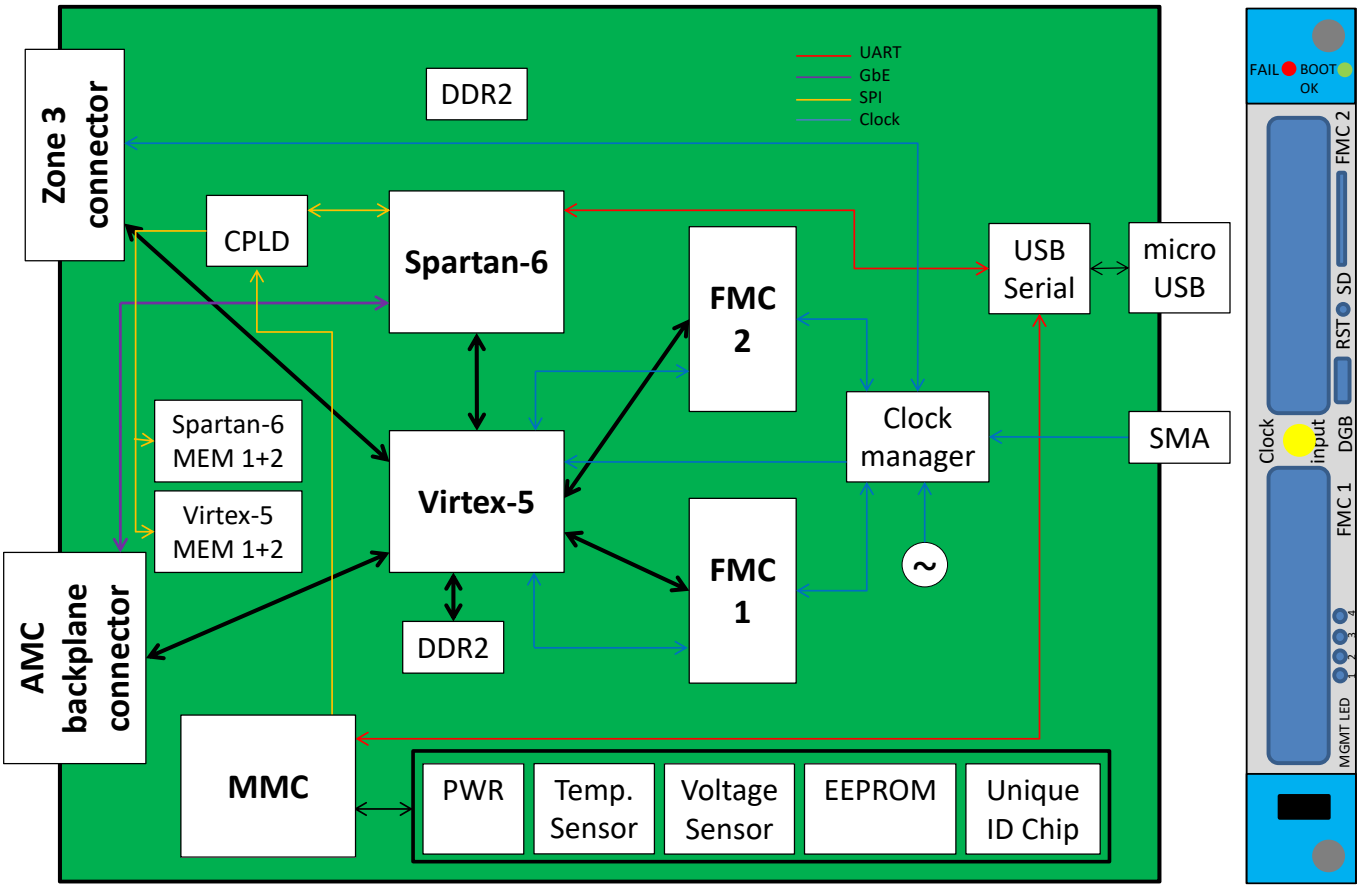
Compliance	RoHS
Licensing to industry	Yes / Deutsches Elektronen-Synchrotron - Notkestr. 85, 22607 Hamburg - Germany - Email: mtca-techlab@desy.de

MicroTCA TECHNOLOGY LAB

DESY.

AMC - Dual HPC-FMC Carrier DAMC-FMC25

FUNCTIONAL BLOCK DIAGRAM AND FRONT PANEL



DESY Deutsches Elektronen-Synchrotron
Notkestr. 85 • 22607 Hamburg
mtca-techlab@desy.de
techlab.desy.de

MicroTCA TECHNOLOGY LAB

DESY.