AMC Data Processing and Telecommunication Module

DAMC-TCK7

HIGHLIGHTS

- Kintex-7 FPGA
- 8 SFP+ slots
- 2 Gigabytes DDR3 SDRAM
- 8 MGT links to backplane

FEATURES

Advanced Mezzanine Card (AMC)
Powerful Kintex-7 FPGA (XC7K355T or XC7K420T)
2 Gigabytes of DDR3 SDRAM
8x SFP+ on front panel (10 Gbps *)
PCIe x4 gen. 3 (8 Gbps)
2 channels of Gigabit Ethernet (1 Gbps)
10 direct low latency connections to backplane (10Gbps*)
4 low latency connections to RTM (10 Gbps *)
LVDS parallel bus to RTM (28 lanes)
Partial reconfiguration and firmware upgrade support
Advanced diagnostic, monitoring and debugging
Options: - XC7K355T-FGG901 - XC7K420T-FGG901
Board Support Package under https://github.com/MicroTCA-Tech-Lab/damc-tck7-fpga-bsp

* possible 12.5 Gbps with Kintex-7 speed grade -3

The AMC-based Controller (DAMC-TCK7) board is a general purpose high-performance low-latency data processing unit designed according to the PICMG MTCA.4 specifications. The module provides processing power, data memory, communication links and reference clock signals. The module was originally designed as a LLRF (Low Level Radio Frequency) cavity field stabilizing controller for standing-wave linear accelerators. However, the application of the board is much wider for systems requiring low latency and high speed digital signal processing.

The Xilinx FPGA (Field Programmable Gate Array) device available on the DAMC-TCK7 board delivers a computing power and memory for low-latency digital signal processing. The FPGA supports a number of Low Latency Links (LLLs) available on the front panel, at the backplane and a Rear Transition Module (RTM) Zone 3 connector, working with a few Gbps throughput.

DESY offers the DAMC-TCK7 for licensing to industry. DESY can modify this product to meet special customer requirements.

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AMC Data Processing and Telecommunication Module
DAMC-TCK7

TECHNICAL SPECIFICATIONS

ARCHITECTURE			
Physical		Dimensions	Double width, Mid-Size with Full-Size option Width: 5.486” (148.5 mm) Depth: 7.110” (180.6 mm)
Standards		MTCA.4	Advanced Mezzanince Card
		Module management	IPMI Version 2.0
Compatibility		Zone 3 classification	Class D1.2
		Compatible RTM products	DRTM-VM2, DRTM-AD84, DRTM-PZT4
CHANNELS			
Type	Data Processing Module	Number of communication channels	28
		Total throughput	350 Gbps
		FPGA resources	Slices: 65, 150, DSP slices: 1,680
Electrical properties		Power consumption	<24 W
		Typical latency	<2 us
Components	FPGA	Xilinx Kintex-7	XC7K355T or XC7K420T
	RAM	DDR3-1066 SDRAM	256 M x 64 bit
	PROM	QSPI FLASH	2 x 256 Mbit
	clock reference	Oscillator	50 MHz
		PLL	2x quad output PLL
		Frequency	30 – 325 MHz
		Jitter	<134 dBc/Hz@1 MHz
		Configuration interface	I²C
CONNECTIVITY			
Front panel	Low latency connection	Front panel	8 channels
		connector type	SFP+ cage, optical fibre
		Data throughput	10 Gbps (12.5 Gbps)
		Bit error rate	$<10^{14}$ bit^{-1}
	Reference clock	Front panel	1 channel
		Connector type	SMA, single-ended
		Impedance/coupling	50 Ω/AC
		Maximum input power level	1 dBm
	Debug interface	Front panel	2 channel, FPGA and MMC
		Connector type	Micro USB
		Data throughput	3 Mbps
Backplane	Low latency connection	Backplane	8 channels
		Interface type	Peer-to-peer, ports 8-15 according to AMC specification
		Data throughput	10 Gbps (12.5 Gbps)
		Bit error rate	$<10^{14}$ bit^{-1}
	Low latency connection	Backplane	2 channels
		Interface type	Peer-to-peer, ports 2-3 according to AMC specification
		Data throughput	10 Gbps
		Bit error rate	$<10^{14}$ bit^{-1}
	PCIe	Backplane	4 lanes
		Interface type	PCIe gen. 3.0
		Data throughput	8 Gbps x 4
		Bit error rate	$<10^{14}$ bit^{-1}
	Gigabit Ethernet	Backplane	2 channels
		Data throughput	1 Gbps

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AMC Data Processing and Telecommunication Module
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TECHNICAL SPECIFICATIONS

CONNECTIVITY (CONTINUED)

Zone 3	Low latency connection	RTM	8 channels
		Connector type	Peer-to-peer, ports 8-15 according to D1.2 digital class
		Data throughput	10 Gbps (12.5 Gbps)
		Bit error rate	$<10^{14}$ bit^{-1}
	Parallel bus	RTM	38 differential pairs
		Connector type	LVDS
		Data throughput	38 Gbps
		Bit error rate	$<10^{14}$ bit^{-1}
	AMC clock	Clock output	2 reference clock signals
		Connector type	LVDS
		Clock frequency	50 … 325 MHz / TCLKA
	RTM clock	Clock input	2 reference clock inputs
		Clock type	FPGA global clock, GTX reference clock, PLL
	Others	MTCA.4 signals	IPMI bus - I²C, presence, power supply
		Interlocks	dedicated output signals
		JTAG	JTAG chain, +3V3

OTHER FEATURES

On board	Power supply management	Via PMBUS
	RTM management	With power supply and curent monitoring
	Firmware upgrade	Yes, via IPMI and PCIe interface
	Voltage and current monitor	Yes, readout via IPMI
	Clock monitoring	Yes, readout via IPMI
	LEDs	IPMI management control
	Mechanical	Hot swap ejector handle
Environmental	Operating temperature	0 … 50 °C
	Storage temperature	-40 … +90 °C
	Relative humidity	5 … 90 %, non-condensing
	Weight	0.7 kg

OTHER

Compliance	RoHS
Licensing to industry	Yes / Deutsches Elektronen-Synchrotron - Notkestr. 85, 22607 Hamburg - Germany - Email: mtca-techlab@desy.de

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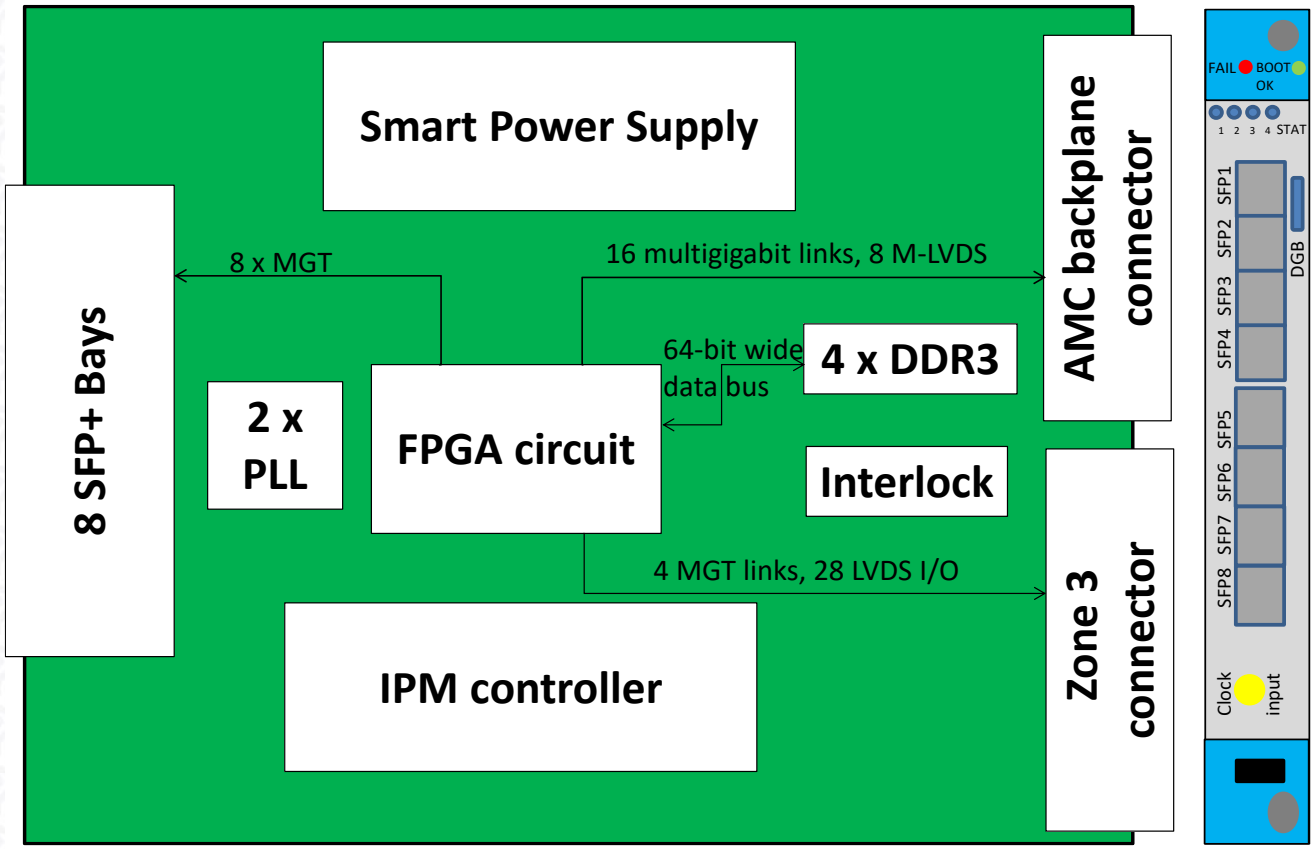
FUNCTIONAL BLOCK DIAGRAM AND FRONT PANEL



OPTIONS

DAMC-TCK7- A - B

	FPGA type
A	355 = XC7K355T
	420 = XC7K420T

	FPGA speed grade
B	1 = speed grade -1
	2 = speed grade -2
	3 = speed grade -3

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