DMMC-STAMP Breakout Board (DMMC-STAMP-BoB)

Pin Headers

X100 RX15_P — GND — DNP
X102 TX15_P — GND — DNP
X104 RX14_P — GND — DNP
X106 TX14_P — GND — DNP
X101 RX15_N — GND — DNP
X103 TX15_N — GND — DNP
X105 RX14_N — GND — DNP
X107 TX14_N — GND — DNP

P2 — TSW-104-07-F-D

RTM_JTAG_TDI	2	1	AMC_JTAG_TMS
RTM_JTAG_TDO	4	3	AMC_JTAG_TCK
GND	6	5	AMC_JTAG_TDI
CPLD_GPIO_IO1	8	7	AMC_JTAG_TDO

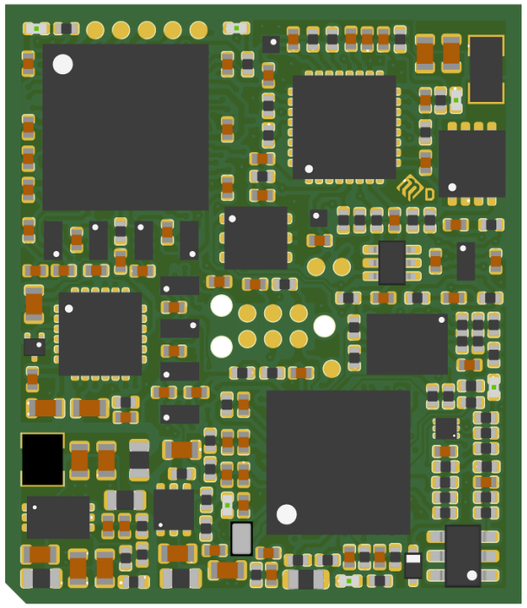
P3 — TSW-104-07-F-D

FPGA1_GPIO_GPIO2	2	1	FPGA1_SPI_MOSI
FPGA1_GPIO_GPIO1	4	3	FPGA1_SPI_MISO
VCC_FPGA1	6	5	FMC2_PRESENCE
FPGA1_GPIO_GPIO7	8	7	FMC1_PRESENCE

X108 FCLK_P — GND — DNP
X110 RX4_P — GND — DNP
X112 TX4_P — GND — DNP
X109 FCLK_N — GND — DNP
X111 RX4_N — GND — DNP
X113 TX4_N — GND — DNP

P4 — TSW-114-07-F-D

MMC_GPIO_IO9	2	1	CPLD_GPIO_IO0
XO2_JTAG_TDO	4	3	XO2_JTAG_TDI
VCC_FPGA2	6	5	FPGA2_JTAG_TCK
FPGA2_JTAG_TDO	8	7	FPGA2_JTAG_TDI
FPGA2_SPI_MISO	10	9	FPGA2_SPI_MOSI
FPGA2_SPI_SCK	12	11	FPGA2_SPI_CSMUX
FPGA2_GPIO_GPIO9	14	13	FPGA2_CTL_PROGN
FPGA2_GPIO_GPIO1	16	15	FPGA2_CTL_DONE
FPGA2_GPIO_GPIO2	18	17	FPGA2_GPIO_GPIO3
FPGA2_GPIO_GPIO5	20	19	FPGA2_GPIO_GPIO6
USB_VTG	22	21	PGND
	24	23	PGND
	26	25	PGND
MMC_GPIO_IO1	28	27	VCC+12V_JPR



P5 — TSW-114-07-F-D

RTM_Z3DRVEN	2	1	MMC_GPIO_IO4
GND	4	3	VCC+12V_PP_RTMIN
FPGA1_GPIO_GPIO9	6	5	FPGA1_SPI_CS
FPGA1_SPI_SCK	8	7	VCC_RTM+3V3_MP
GND	10	9	VCC_RTM+12V
FPGA1_GPIO_GPIO3	12	11	FPGA1_GPIO_GPIO4
FPGA1_GPIO_GPIO5	14	13	FPGA1_GPIO_GPIO6
RTM_I2C_SCL	16	15	RTM_I2C_SDA
FMC_I2C_SCL	18	17	FMC_I2C_SDA
IPMB-L_I2C_SCL	20	19	IPMB-L_I2C_SDA
IPMI_HANDLE	22	21	IPMI_ENABLE_N
IPMI_GA1	24	23	IPMI_GA2
IPMI_PS0_N	26	25	IPMI_GA0
GND	28	27	IPMI_PS1_N

P6 — TSW-114-07-F-D

GND	2	1	CPLD_GPIO_IO2
XO2_JTAG_TCK	4	3	XO2_JTAG_TMS
FPGA2_JTAG_TMS	6	5	FPGA1_GPIO_GPIO8
FMC1_JTAG_TDI	8	7	FMC1_JTAG_TDO
FMC1_JTAG_TCK	10	9	FMC1_JTAG_TMS
FPGA2_SPI_DRVEN	12	11	FPGA2_SPI_CS
FPGA2_CTL_INITN	14	13	GND
FPGA2_CTL_RST	16	15	FPGA2_TXD
FPGA2_GPIO_GPIO4	18	17	FPGA2_RXD
FPGA2_GPIO_GPIO7	20	19	FPGA2_GPIO_GPIO8
CPLD_GPIO_IO3	22	21	MMC_GPIO_IO2
MMC_GPIO_IO0	24	23	MMC_GPIO_IO3
MMC_GPIO_IO8	26	25	GND
MMC_GPIO_IO5	28	27	VCC+3V3_MMC

P7 — TSW-114-07-F-D

RTM_JTAG_TCK	2	1	RTM_JTAG_TMS
FPGA1_JTAG_TCK	4	3	FPGA1_JTAG_TMS
FPGA1_JTAG_TDI	6	5	FPGA1_JTAG_TDO
PMBUS_I2C_SDA	8	7	FPGA1_SPI_DRVEN
FPGA1_SPI_CSMUX	10	9	PMBUS_I2C_SCL
MMC_GPIO_IO7	12	11	FPGA1_CTL_RST
MMC_GPIO_IO6	14	13	FPGA1_CTL_DONE
RTM_PS_N	16	15	FPGA1_CTL_INITN
VCC+3V3_MP_JPR	18	17	FPGA1_CTL_PROGN
FPGA1_RXD	20	19	FPGA1_TXD
FMC2_PG_C2M	22	21	FMC2_PG_M2C
FMC1_PG_C2M	24	23	FMC1_PG_M2C
SWD_CLK	26	25	RST_B
SENS_I2C_SDA	28	27	SENS_I2C.SCL

Rev. C: new

X92 — 1 VCC+12V_PP_RTMIN — 2 GND — DNP
X93 — 1 VCC_RTM+12V — 2 GND — DNP

P8 — TSW-104-07-F-D

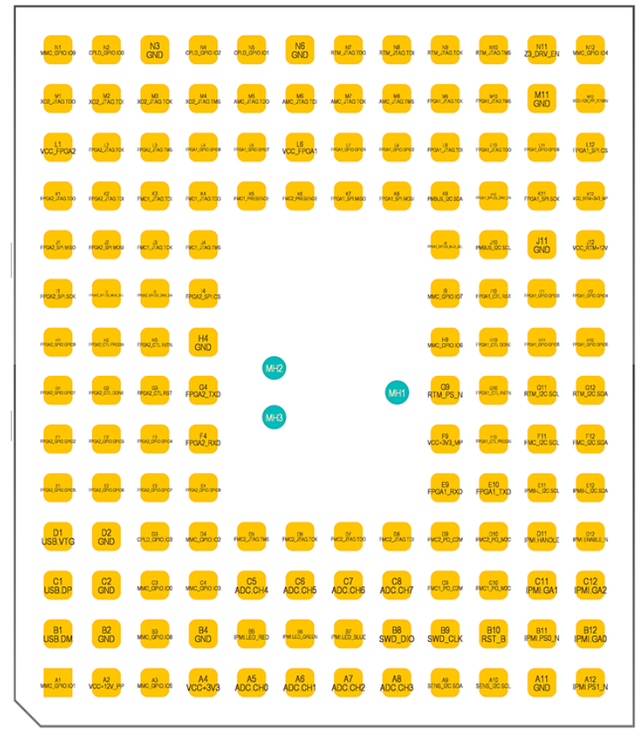
FMC2_JTAG_TDI	2	1	ADC_CH7
FMC2_JTAG_TDO	4	3	ADC_CH6
FMC2_JTAG_TCK	6	5	ADC_CH5
FMC2_JTAG_TMS	8	7	ADC_CH4

P9 — TSW-104-07-F-D

SWD_DIO	2	1	ADC_CH3
IPMI_LED_BLUE	4	3	ADC_CH2
IPMI_LED_GREEN	6	5	ADC_CH1
IPMI_LED_RED	8	7	ADC_CH0

Tag Connect TC2030 Plug (on LGA Module)

LGA Footprint (Top View)



Debug Jumpers (Standalone Operation)

Caution: Voltages can be shorted here. Read the manual!

IPMI_ENABLE_N — J8 — GND
VCC+3V3_MMC — J9 — VCC+3V3_MP_JPR

Extra GND

GND — J1 — DNP — GND
GND_0R — J13 — DNP — GND_0R

0R Bridges for to optional MTCA.4 Module

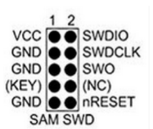
FPGA1_SPI_CS	0	R90	FPGA1_SPI_CS_0R	
FPGA1_SPI_CSMUX	0	R42	FPGA1_SPI_CSMUX_0R	
FPGA1_SPI_MISO	0	R43	FPGA1_SPI_MISO_0R	
FPGA1_SPI_MOSI	0	R44	FPGA1_SPI_MOSI_0R	
FPGA1_SPI_SCK	0	R45	FPGA1_SPI_SCK_0R	
RTM_PS_N	0	R46	RTM_PS_N_0R	
RTM_I2C_SDA	0	R47	RTM_I2C_SDA_0R	
RTM_I2C_SCL	0	R48	RTM_I2C_SCL_0R	
RTM_JTAG_TCK	0	R49	RTM_JTAG_TCK_0R	
RTM_JTAG_TDO	0	R50	RTM_JTAG_TDO_0R	
RTM_JTAG_TDI	0	R51	RTM_JTAG_TDI_0R	
RTM_JTAG_TMS	0	R52	RTM_JTAG_TMS_0R	
VCC_FPGA1	0	R53	VCC_FPGA1_0R	
VCC+3V3_MMC	0	R54		
	0	R59	VCC+3V3_MMC_0R	
VCC+3V3_MP	0		VCC+3V3_MP_0R	
PMBUS_I2C_SCL	0	R57	PMBUS_I2C_SCL_0R	
PMBUS_I2C_SDA	0	R58	PMBUS_I2C_SDA_0R	
VCC_RTM+3V3_MP	0	R55	VCC_RTM+3V3_MP_0R	
VCC_RTM+12V	0	R56	VCC_RTM+12V_0R	HCJ1206ZT0R00
	0	R60		
VCC+12V_PP	0	R61	VCC+12V_PP_0R	
GND		R62	GND_0R	HCJ1206ZT0R00
GND			GND_0R	HCJ1206ZT0R00
GND		R91	GND_0R	HCJ1206ZT0R00
ESD_SEGMENT3	0	R92	ESD_SEGMENT3_0R	

MCU JTAG Port (optional, MMC-STAMP has on-board JTAG "plug of nails" socket)

VCC+3V3_MP — X7 — GND — 3220-10-0200-00

1	2	SWD_DIO	
3	4	SWD_CLK	
5	6	SWO	
TRST 7	8	N.C.	
9	10	RST_B	

Name	AVR port pin	SAM port pin	Description
SWDCLK	1	4	Serial Wire Debug Clock.
SWDIO	5	2	Serial Wire Debug Data Input/Output.
SWO	3	6	Serial Wire Output (optional- not implemented on all devices).
nSRST	6	10	Reset.
VTG	4	1	Target voltage reference.
GND	2, 10	3, 5	Ground.



Current Measurement Jumpers

VCC+12V_PP — J2 — VCC+12V_PP_RTMIN
VCC+12V_PP — J4 — VCC+12V_JPR
VCC+3V3_MP — J3 — VCC+3V3_MP_JPR
PGND — J5 — GND
PGND — J6 — GND
PGND — J7 — GND

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Project Title: **dmmc-stamp-bo-revd.prjpcb**
Schematic Title: **LGA Footprint (2mm pitch)**
DATE: 19.04.2024 13:28:15

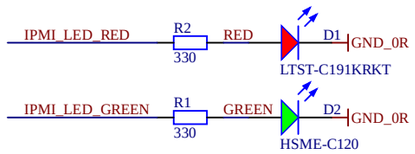
Engineer 1: Michael Feniner
Engineer 2: S. Chystiakov / J.Zink

FILENAME: Debug.SchDoc

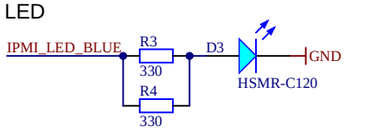
Rev: D
Size: A3
Sheet: 1 of 3

Mandatory Components on AMC Card

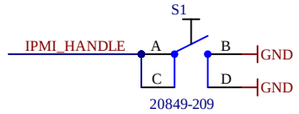
IPMI LEDs (fault / OK)



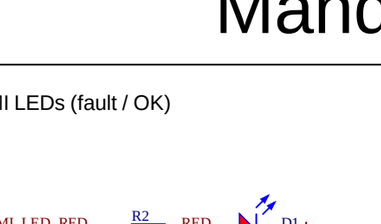
Blue LED



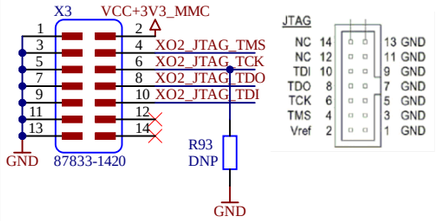
MicroTCA Handle Dummy



USB Debug Connector (recommended)



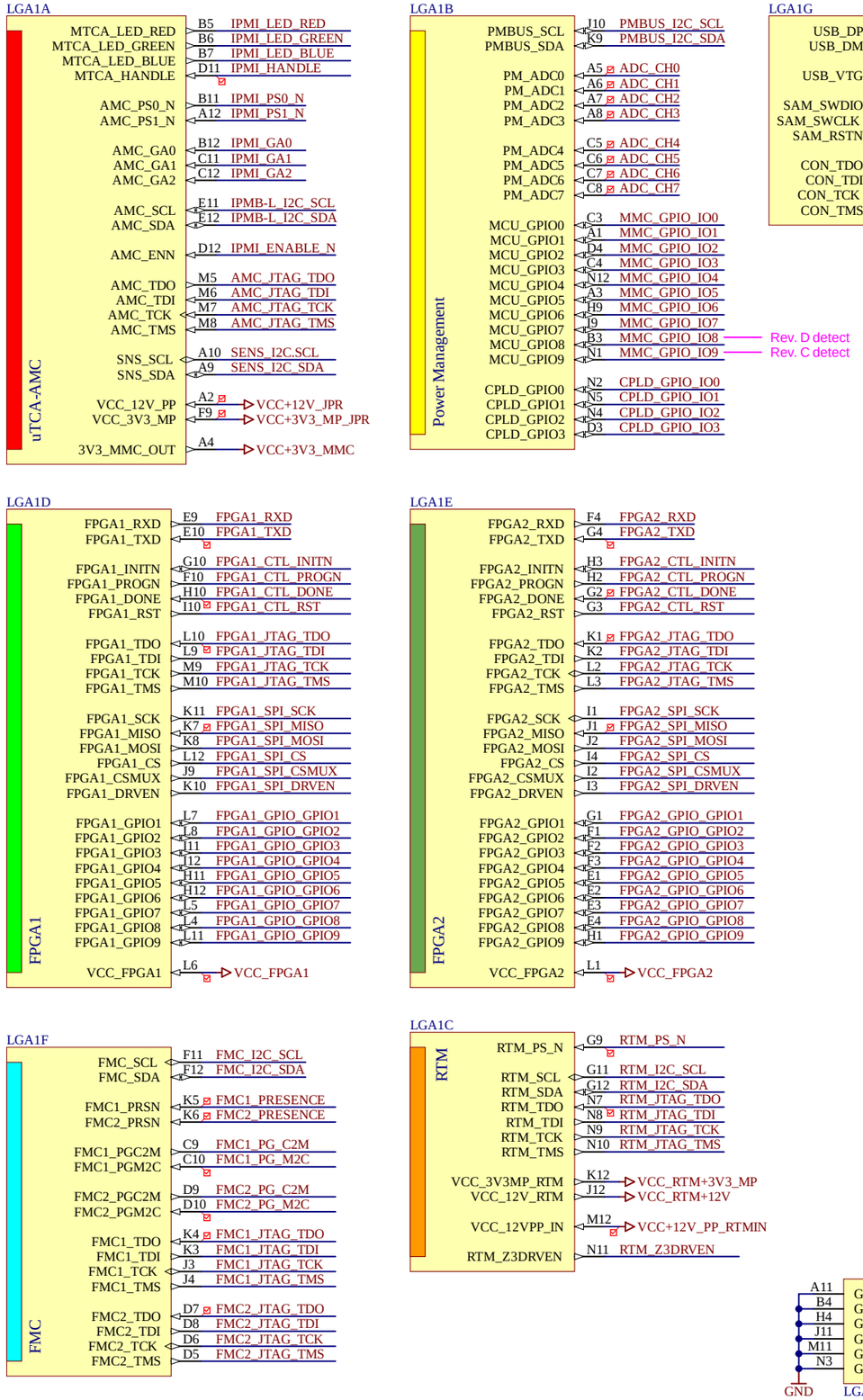
Xilinx JTAG IN (recommended)



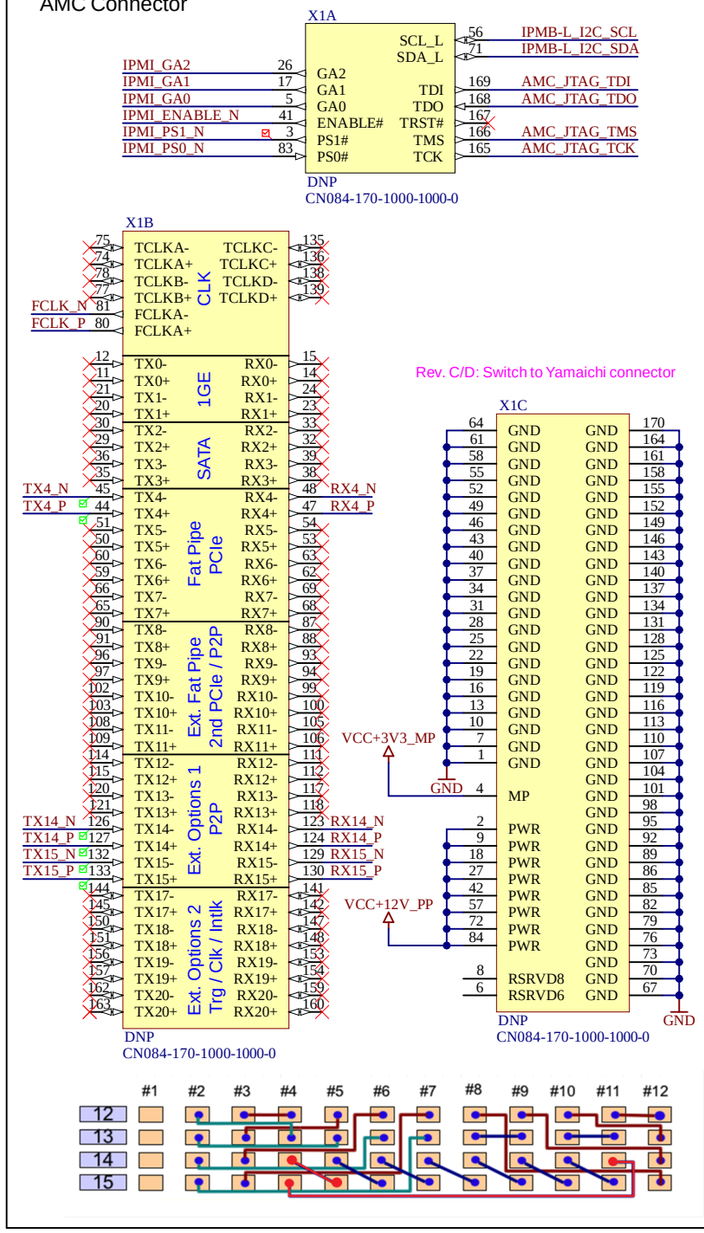
During a short moment on power-up, the CPLD on the MMC Stamp is in in-system programming mode where the firmware can be updated using this JTAG interface*. In corner cases, noise on the JTAG lines can be caught by the CPLD and accidently bring it into JTAG debug mode, where it does not respond to user commands anymore until the next power cycle. After power-up, the CPLD is in JTAG-forward mode and prevents any noise by activating integrated pull-ups. The pull-down resistor installed on the board will prevent that any unwanted noise is interpreted as JTAG commands. This bevaiour was adressed with revision C of the MMC Stamp. Only the prototypes that are used on BoB are sentivie to this corner case. Any Stamps delivered to customers do not need this fix.

*During normal operation, the CPLD is in-system-updated by MMC software and not via JTAG.

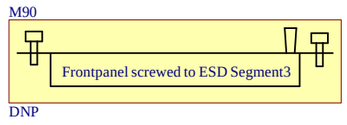
MMC Stamp LGA Module



AMC Connector



Front Panel



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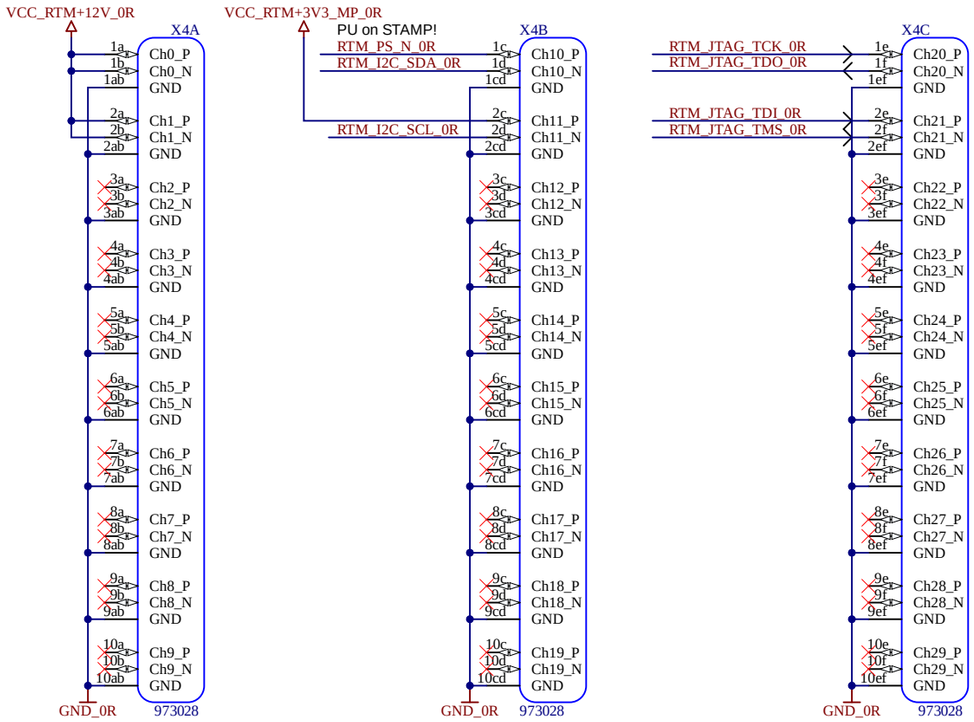
Project Title:
dmmc-stamp-bo-revd.prjpcb
Schematic Title:
Mandatory Components
DATE: 15.05.2024 13:28:15

Engineer 1: Michael Feniner
Engineer 2: S. Chystiakov / J.Zink

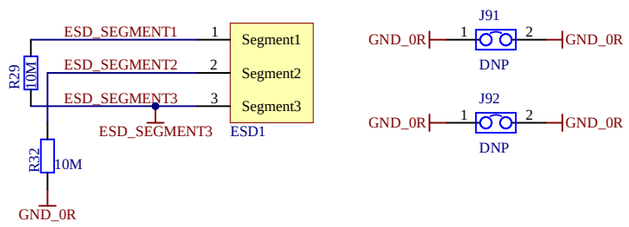
Rev: D
Size: A3
Sheet: 2 of 3

FILENAME: Mandatory.SchDoc

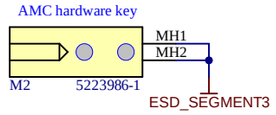
Zone 3 Power, Management, JTAG (optional)



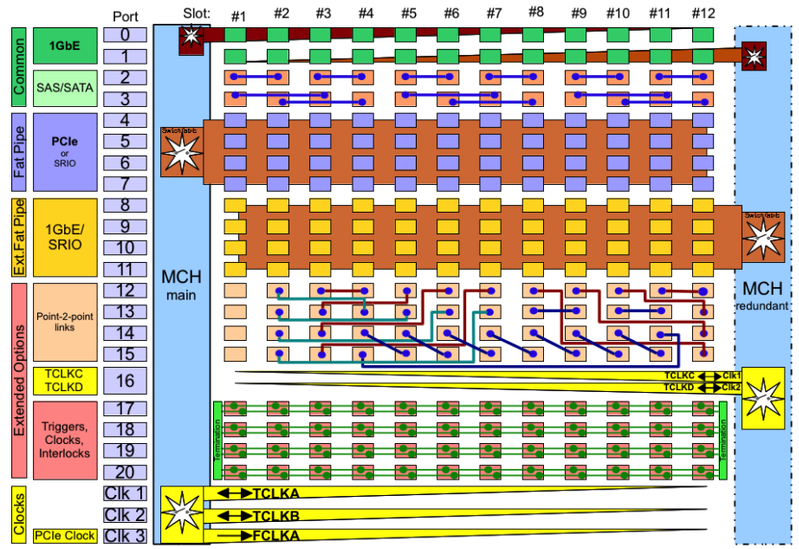
ESD Strip

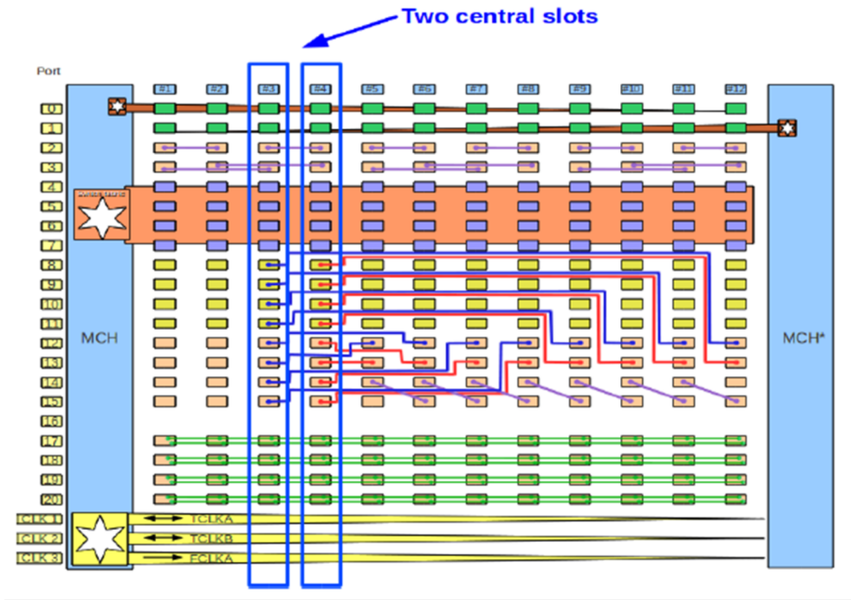


Zone 3 Key

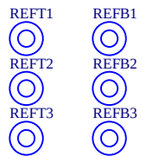


For Information: Typical Backplane Topologies





Fiducials



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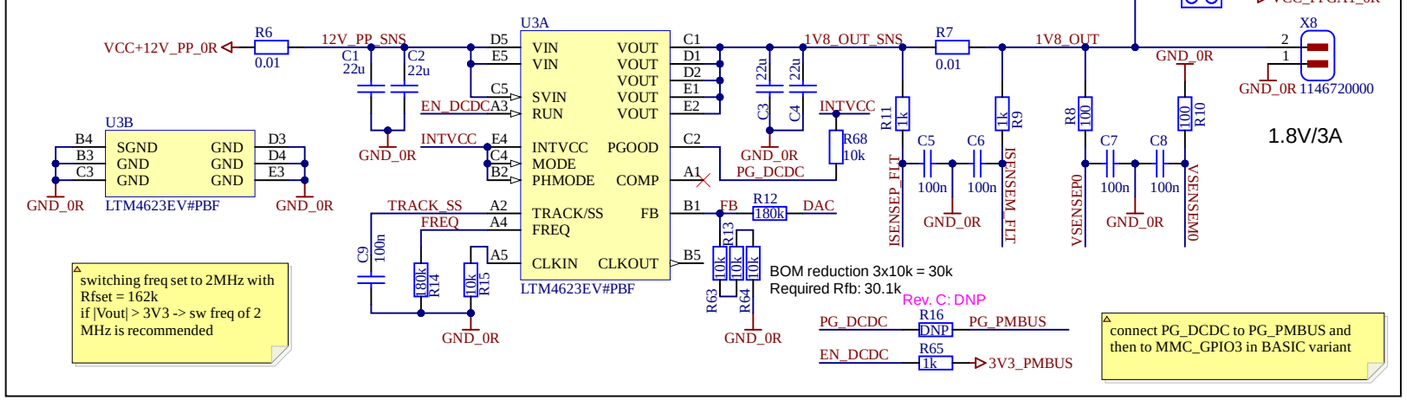
Project Title:
dmmc-stamp-bo-revd.prjpcb
Schematic Title:
Optional Components
DATE: 19.04.2024 13:28:15

Engineer 1: Michael Feniner
Engineer 2: S. Chystiakov / J.Zink
FILENAME: zone3.SchDoc

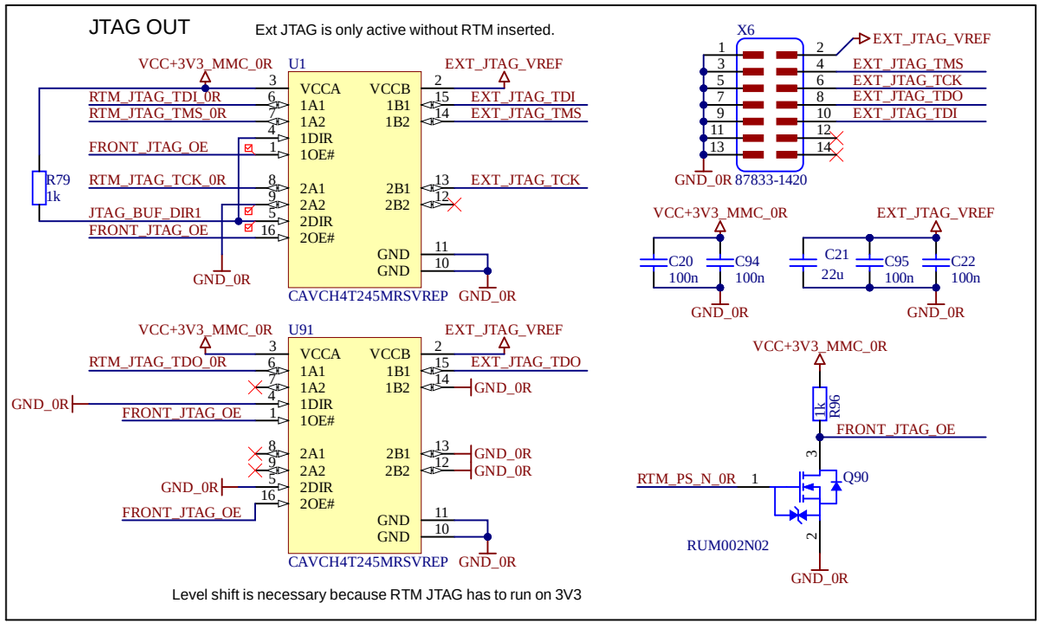
Rev: D
Size: A3
Sheet: 3 of 3

Example Periperals: Power, PMBUS(TM), Flash, FPGA JTAG, Zone3

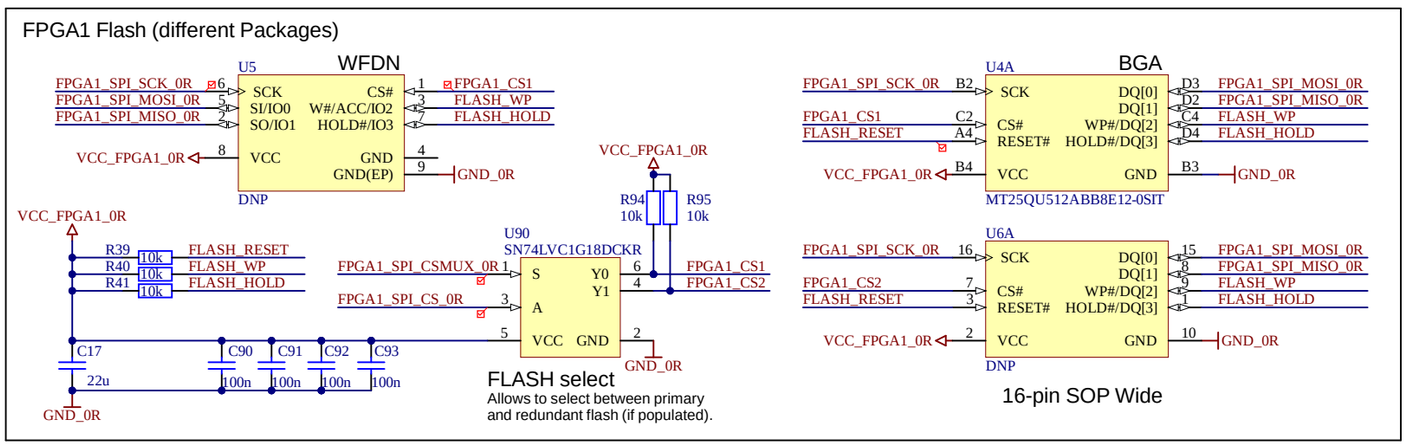
Example 2: Low EMI 3A uModule(TM) DCDC Converter (2)



JTAG OUT

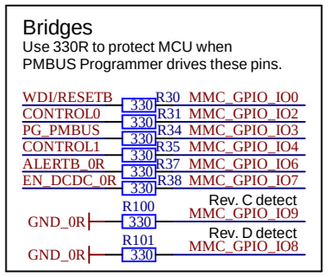


FPGA1 Flash (different Packages)

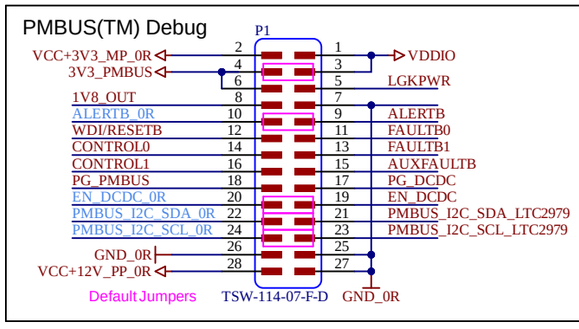


Bridges

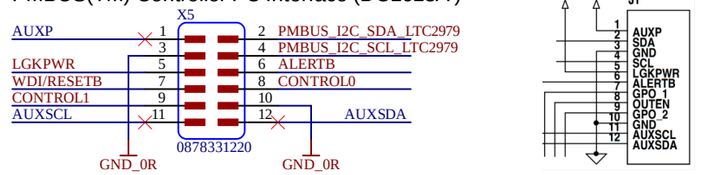
Use 330R to protect MCU when PMBUS Programmer drives these pins.



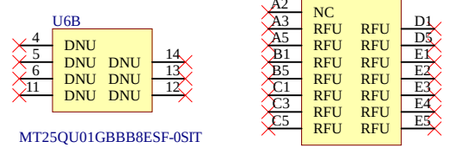
PMBUS(TM) Debug



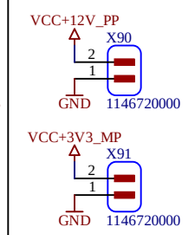
PMBUS(TM) Controller PC Interface (DC1613A)



Unused sub-parts



External Power In



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Project Title:
dmmc-stamp-bo-revd.prjpcb
Schematic Title:
Optional Components
DATE: 15.05.2024 13:28:16

Engineer 1: Michael Feniner
Engineer 2: S. Chystiakov / J.Zink

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Rev: D
Size: A3
Sheet: 3 of 3