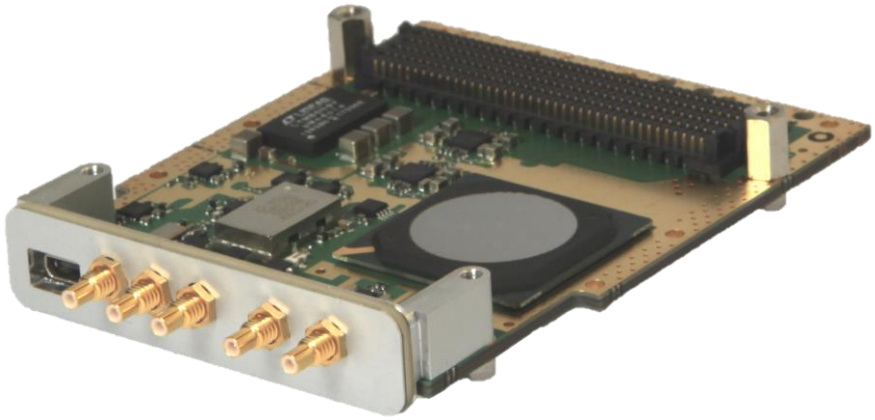
High Speed Direct Sampling FMC

DFMC-DS800 / DFMC-DS500

HIGHLIGHTS

- Single-channel ADC with up to 1.6 GSPS or dual-channel up to 800 MSPS operation
- Up to 6 trigger inputs / GPIO outputs
- AC-/ DC-coupled inputs



FEATURES

Single Size FPGA mezzanine card (FMC)
ANSI/VITA 57.1 standard compliant HPC (high pin count module)
12-bits, 500/800 MSP/s dual-channel ADC, 1000/1600 GSPS single-channel ADC
ADC analogue input bandwidth: >2.5 GHz
Amplifier LS bandwidth: 4.8 GHz with AC- / DC-coupled inputs
Ext. clock input connector, high stability TCXO, ultra-low phase noise PLL with VCSO on-board
8.5 mm stacking height, air cooled
front panel: 5 RF SSMC + 1 HDMI Type D (micro) connectors
Up to 6 Trigger / GPIO signals (4 LVDS differential + 2 single ended 3.3V)
User EEPROM for calibration data
RoHS compliant

The DFMC-DS500/800 is a FPGA mezzanine card (FMC) carrying a mid to high speed digitizer. It is fully ANSI/VITA 57.1 compliant. The FMC has a high pin count connector with a stacking height of 8.5mm and therefore it is fully air cooled.

The FMC offers a dual channel 12-bit ADC with 500/800 MSPS. There are also variants with up to 1.6 GSPS per channel and 10-bits resolution available. The DS500/800 supports AC and DC single-ended input signals with a level up to $1V_{p\text{-}p}$. The input bandwidth is >2.5 GHz (TBD). The digital interfaces to the FPGA are 2x 13-bits parallel LVDS lines.

Versatile clocking options are offered by the DS500/800. ADC clock is fed in directly via a front panel connector. There is a high-precision TCXO combined with a multi loop PLL on the board available. The PLL consists of an ultra-low phase noise VCSO and a custom-build loop filter. A clock monitoring output is also located at the front panel.

For triggering there are 4 LVDS and 2 single ended inputs on the front panel. These trigger signals can be configured as general purpose inputs and outputs.

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High Speed Direct Sampling FMC DFMC-DS800

TECHNICAL SPECIFICATIONS

ARCHITECTURE

Physical	Dimensions	Single-width 8.5mm stacking height, air cooled
		Regions 1,2 and 3 occupied
		Size: 84 x 69 mm
Standards	ANSI/VITA 57.1	FPGA mezzanine card (FMC)
	FMC classification	HPC
Compatibility	Compatible products	DAMC-FMC2ZUP, DAMC-FMC1Z7IO
		DAMC-FMC25, DAMC02, DAMC-TCK7, DAMC02
		ANSI/VITA 57.1 carriers, KCU105, KCU116

CONFIGURATION

Type	Analog to Digital converter	Number of channels	2
Electrical properties		Power consumption	max. 7W (over FMC Connector)
		ADC	12-bit, dual channel with 500 / 800 MSP/s, single channel 1.0 / 1.2 GSP/s
			> 2.4 GHz input bandwidth
			max. input level: 1Vp-p
		PLL	TCXO connected to PLL as reference input,custom made loop filter with ext. low phase noise VCSO
			TCLKA connected from FMC to PLL as reference input

CONNECTIVITY

Inputs/Outputs	Clock	ADC clock input
		Reference clock input
		Clock monitoring output
	Trigger / GPIO	4 differential and 2 single ended gpios
	Connector type	SSMC male connector(HF, Clock), HDMI Type D (IO)

OTHER FEATURES

On board	User I2C interface	to user EEPROM
	PLL	with VCSO and Loop Filter
	TCXO	10 MHz
	VCSO	500 / 800 MHz
	LVDS Transceiver	Trigger / GPIO
Environmental	Operating temperature	0 … 70 °C
	Storage temperature	- 40 … + 90 °C
	Relative humidity	5… 90 %, non-condensing
	Weight	0.3 kg

OTHER

Compliance	RoHS
Standards	ANSI/VITA 75.1
Licensing to industry	Yes / Deutsches Elektronen-Synchrotron - Notkestr. 85, 22607 Hamburg - Germany - Email: mtca-techlab@desy.de

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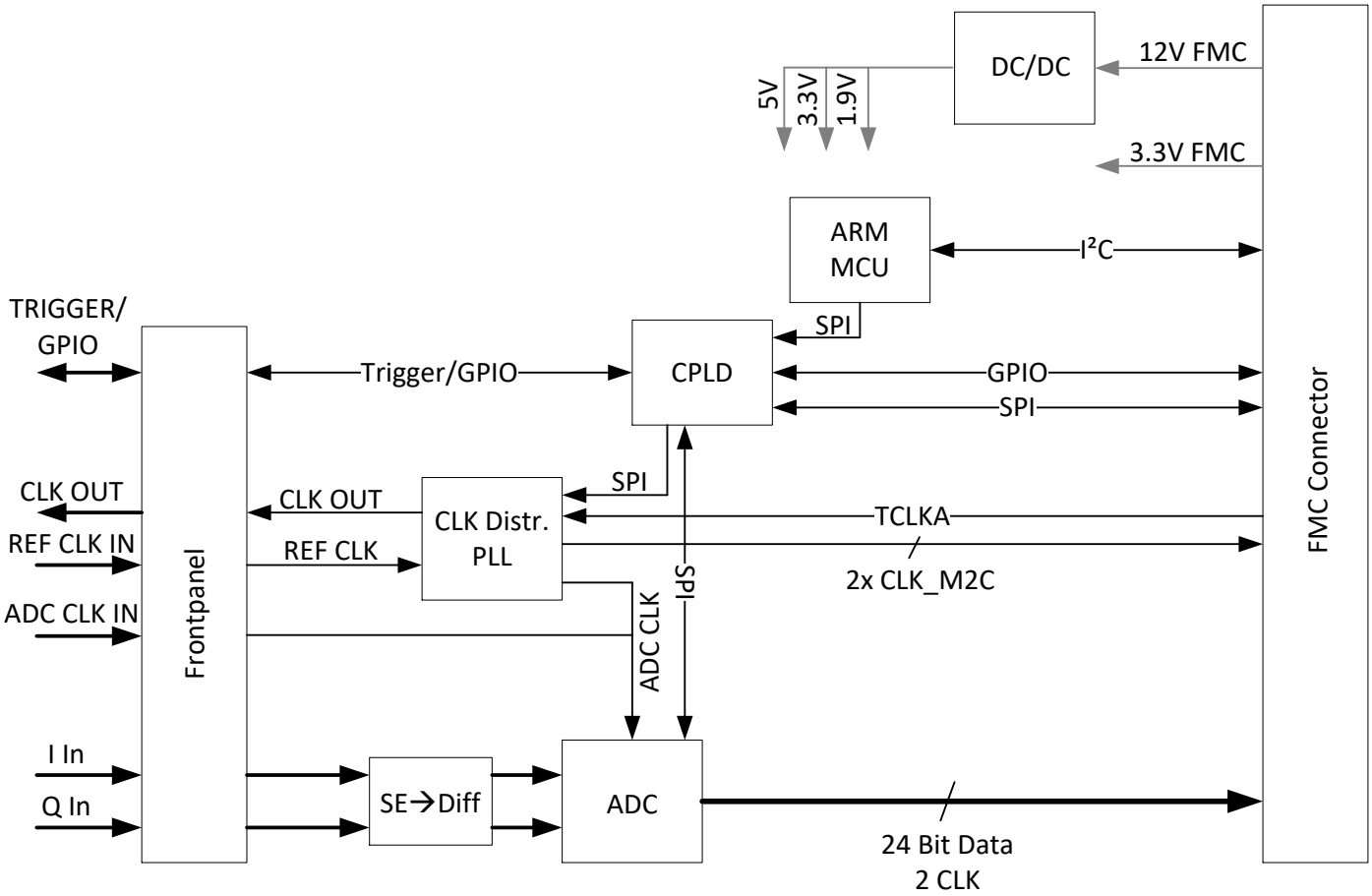
High Speed Direct Sampling FMC DFMC-DS800

FUNCTIONAL BLOCK DIAGRAM AND FRONT PANEL



OPTIONS

DFMC-DS800, DFMC-DS500

DS800	ADC: ADC12D800RF, Sampling rate 1.6 GSPS
DS500	ADC: ADC12D500RF, Sampling rate 1.0 GSPS

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