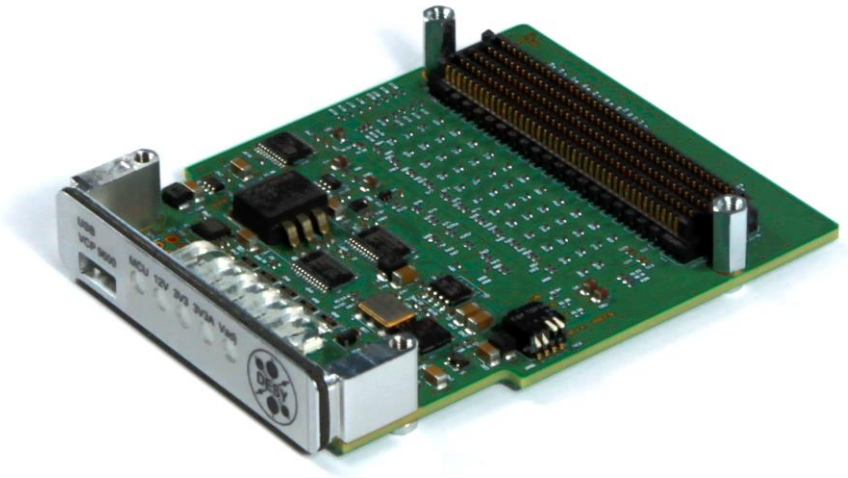
FMC Loopback Adapter

DFMC-TESTADP

HIGHLIGHTS

- Loopback of all LVDS and MGT signals
- 5 RGB LEDs on front panel for power good indication
- 10-280 MHz Oscillator
- MCU for stand-alone operation
- Debug output via USB Interface



FEATURES

FMC form factor

- High pin count interface (HPC)
- FMC clock generator
- FMC HA, HB and LA differential pairs loopbacks
- FMC DP differential pairs loopbacks
- 8-channel ADC for checking supply voltages
- All signals can be checked (including JTAG, Power Good...)

The DFMC-TESTADP is an FPGA Mezzanine Card (FMC) for testing FMC Carriers. It is a tool for carrier developers for testing the full characteristics and connectivity of their FMC carrier interface. The TESTADP features loopbacks on all FMC differential pairs on the HPC connectors. In addition, it provides an on-board, user-programmable low-jitter clock generator supporting reference clocks which are required for PCIe, SATA, SRIO, Fiber Channel or Gigabit Ethernet protocols. It checks also the supply voltage of the FMC carrier connections.

Applications:

- FMC carrier board testing during development or post-production
- FMC carrier board electrical validation

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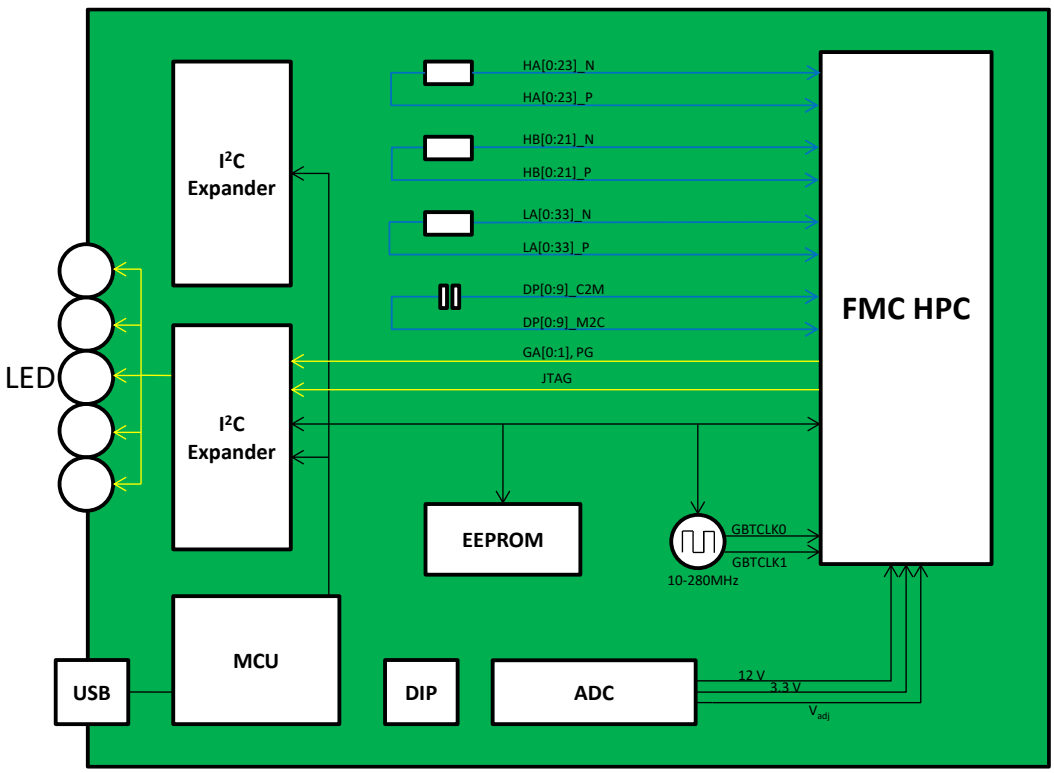
FMC Loopback Adapter DFMC-TESTADP

TECHNICAL SPECIFICATIONS

ARCHITECTURE			
Physical		Width	84 mmm
Standards		FMC Standdard (VITA 57.1)	FPGA Mezzanine Card (FMC)
		module management	IPMI Version 2.0
Compatibility		Compatible products	any standard-compliant FMC carrier
CONFIGURATION			
Electrical properties		VAUX	3.3 V
		VADJ	1.8 V, 2.5 V, 3.3 V
CONNECTIVITY			
Inputs/Outputs	Differiential pairs	HA	24 pairs
		HB	22 pairs
		LA	34 pairs
	Multi-Gigabit Transceivers	DP	10 pairs
	Clock (LVDS)	Chip type Si570	10 - 280 MHz
	Other signals	JTAG	via expander
		Power Good (PG)	PG_M2C, PG_C2M
	Voltages	ADC	3.3 V AUX, 3.3 V, 12 V, VADJ

FUNCTIONAL BLOCK DIAGRAM



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