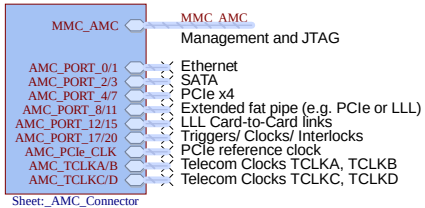
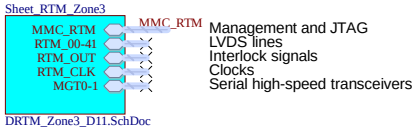
DESY MicroTCA™.4 / 4.1 AMC Implementation Proposal

Draft

AMC Connector (Backplane)



RTM Connector



Altium Designer® Board Template

The schematics and PCB design files are provided free-of-charge. Please contact DESY.

Information

This is an example AMC implementation proposal according to MicroTCA™.4 / 4.1

By publishing recommendations, DESY aims to ease the design of custom MicroTCA™ boards. This solution bases on the DESY MMC Stamp, which was designed to allow fast development of MicroTCA™ boards with maximum interopability between different components.

The MMC Stamp is delivered pre-programmed and is intended to avoid any managment firmware development by the user. If AMC developers wish to vendor-specific management extensions, they can be realized by licensing the MMC Software Development Kit.

Always cross-check with the MicroTCA™ standard. If in doubt, higher priority shall be given to the standard.

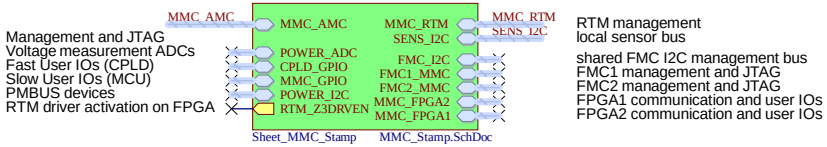
The user is responsible to verify that all implementation details fit to his design requirements.

Disclaimers apply for warranties and limitation of liability. Please check the license terms for more information.

License

DMMC-STAMP LGA Module

Detailed information about DMMC-STAMP can be found here:
https://innovation.desy.de/technologies/microtca/mmc/index_eng.html

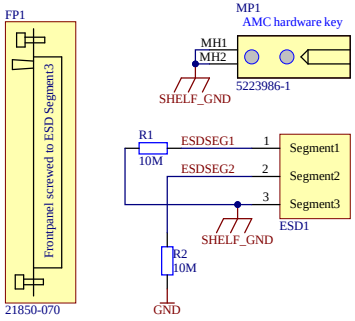


Fiducials (recommended)

List of Changes

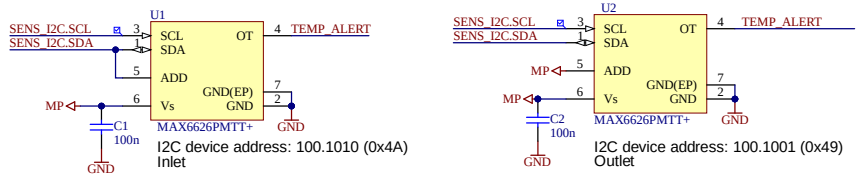
V0.1 - initial revision
V0.2 - spelling corrections; license set to "TBD"
V0.3 - modified FPGAx_CS pin direction, added comments for FPGAx SPI and 3V3_MMC_OUT signals.
V0.4 - general visual beautifications; added note regarding Harting/ITB obsolescence; updated PCB components from valut database, improved front panel mechanics; updated PCB rules to pass DRC
V0.5 - introduction of Yamaichi™ connector; modification of PCB outline
V0.6 - Place outline dimensionioning as defined in standard; unify arcs and corners in outline milling. (diff. with standard was approx. 0.006mm)
V0.7pre - Add gold plating requirements from Yamaichi™; update URLs of Z3 Class definitions; remove 3D models; add 4.1 wording; apply CC BY License
V0.7 - add CC-license compatible 3D modes to all parts.
V0.8 - Change Yamaichi™ layout (improved signal integrity); add milling instructions; add more info on FMC I2C; correct blue LED 3D model; correct I2C address table for inlet/outlet sensors

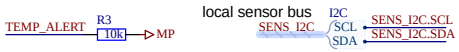
MicroTCA™ Mechanics



Temperature Sensors (mandatory according to MTCA™ standard)

DMMC-STAMP already contains one MAX6626 temperature sensor.



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SENS_I2C address map

0x48 100.1000 Temperature Sensor on stamp
0x49 100.1001 Outlet Temperature Sensor
0x4A 100.1010 Inlet Temperature sensor
```

MAX6626 I2C Address Options

ADD CONNECTION	I²C-COMPATIBLE ADDRESS
GND	100 1000
V_S	100 1001
SDA	100 1010
SCL	100 1011

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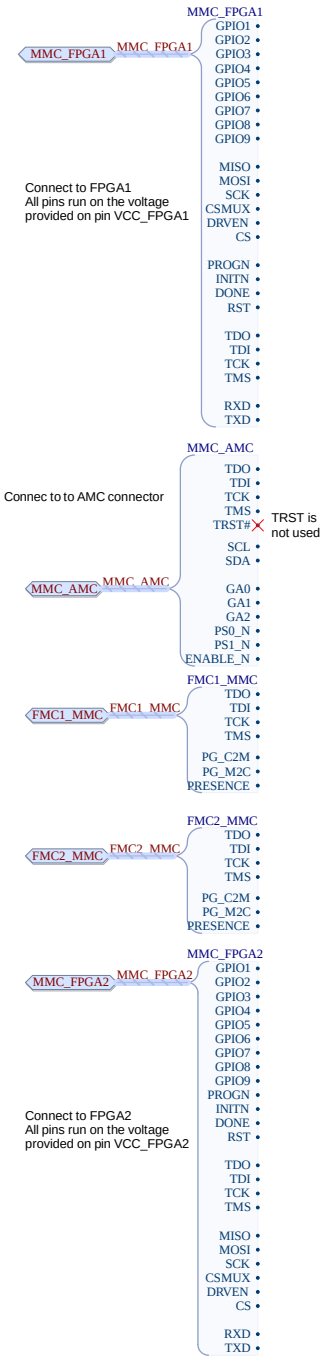
Project Title: **MTCA_AMC-Template.PrjPcb**
Schematic Title: **AMC Template Top**
DATE: 24.01.2025 22:56:08

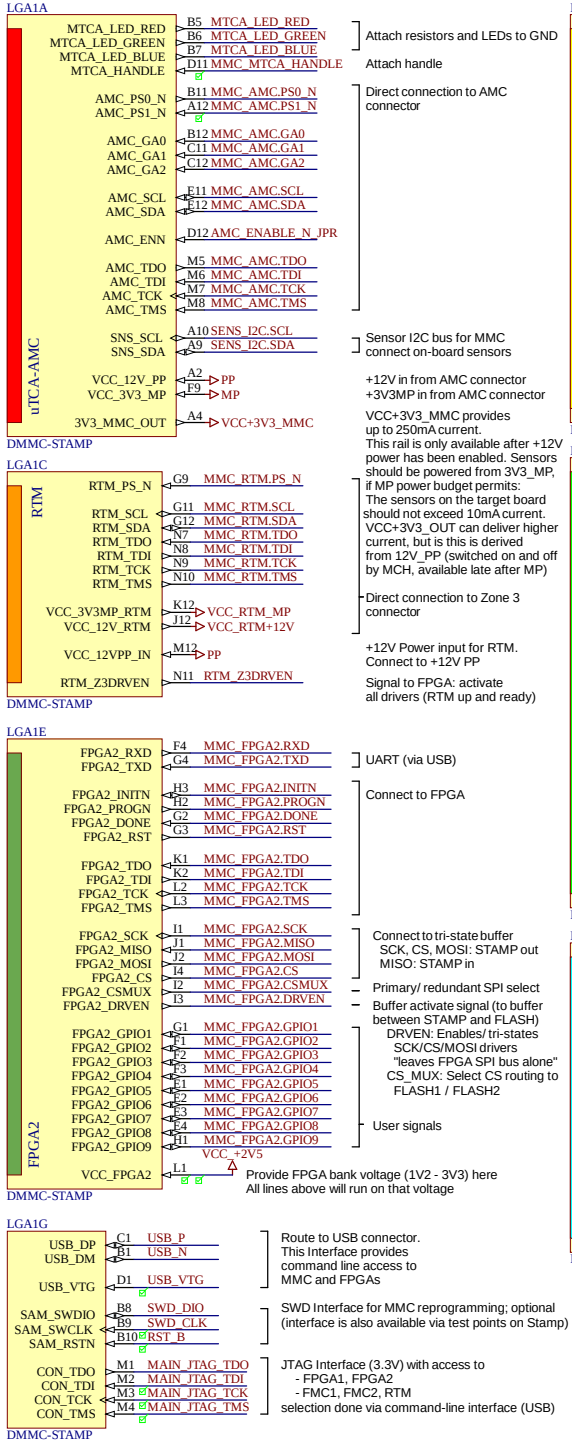
Engineer 1: Michael Fenner
Engineer 2: Robert Wedel

Rev: 0.8
Size: A3
Sheet: 1 of 4

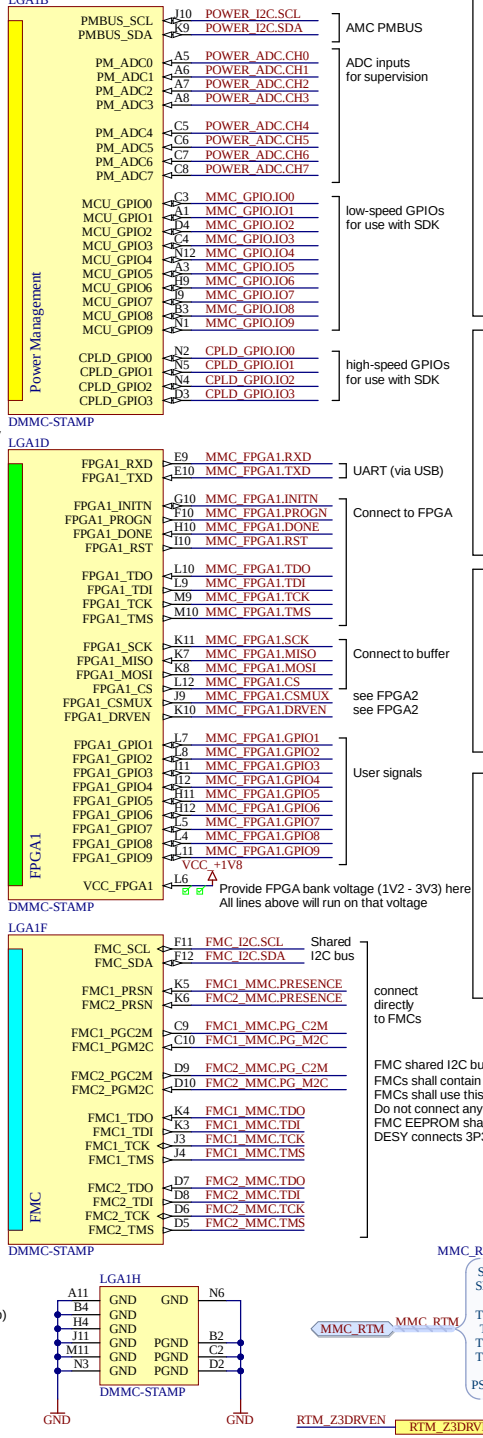
FILENAME: MTCA_AMC-Template_Top.SchDoc

DESY SoM LGA DMMC-STAMP





Attach resistors and LEDs to GND
Attach handle
Direct connection to AMC connector
Sensor I2C bus for MMC connect on-board sensors
+12V in from AMC connector
+3V3MP in from AMC connector
VCC+3V3_MMC provides up to 250mA current. This rail is only available after +12V power has been enabled. Sensors should be powered from 3V3_MP, if MP power budget permits: The sensors on the target board should not exceed 10mA current. VCC+3V3_OUT can deliver higher current, but is this is derived from 12V_PP (switched on and off by MCH, available late after MP)
Direct connection to Zone 3 connector
+12V Power input for RTM. Connect to +12V PP
Signal to FPGA: activate all drivers (RTM up and ready)
UART (via USB)
Connect to FPGA
Connect to tri-state buffer SCK, CS, MOSI: STAMP out MISO: STAMP in
Primary/ redundant SPI select
Buffer activate signal (to buffer between STAMP and FLASH)
DRVEN: Enables/ tri-states SCK/CS/MOSI drivers "leaves FPGA SPI bus alone"
CS_MUX: Select CS routing to FLASH1 / FLASH2
User signals
Provide FPGA bank voltage (1V2 - 3V3) here
All lines above will run on that voltage
Route to USB connector. This Interface provides command line access to MMC and FPGAs
SWD Interface for MMC reprogramming; optional (interface is also available via test points on Stamp)
JTAG Interface (3.3V) with access to
- FPGA1, FPGA2
- FMC1, FMC2, RTM
selection done via command-line interface (USB)

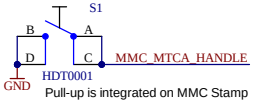


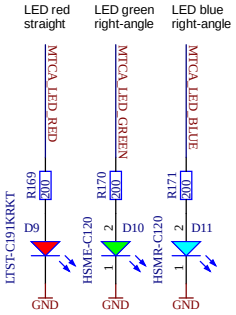
AMC PMBUS
ADC inputs for supervision
low-speed GPIOs for use with SDK
high-speed GPIOs for use with SDK
UART (via USB)
Connect to FPGA
Connect to buffer
see FPGA2
see FPGA2
User signals
Provide FPGA bank voltage (1V2 - 3V3) here
All lines above will run on that voltage
Shared I2C bus
connect directly to FMCs

MTCA™ components - mandatory

Handle and LEDs are mandatory according to AMC Standard.

MTCA Handle



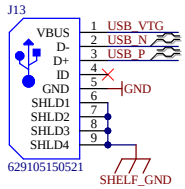


USB Virtual COM Port - highly recommended

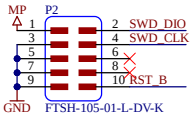
The virtual COM port is highly recommended.
It provides a command-line interface to the MMC Stamp
Via this interface board configuration is done.

The UART of up to two FPGAs are accessible using this interface.

In addition, this interface can be accessed in a Serial-over-LAN-like mode via IPMI.



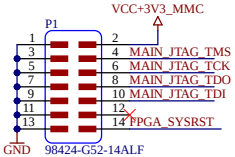
MCU Debug (ARM) - optional (mandatory when using SDK)



MMC Stamp Debug connector is recommended.
When designing own firmware via SDK, it is mandatory.
The MMC stamp always contains SWD test points on the module.

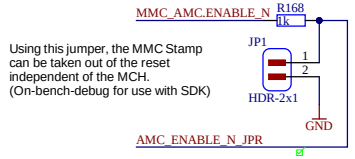
Xilinx™ JTAG IN - recommended

Access to 2 FPGAs, RTM and FMC.

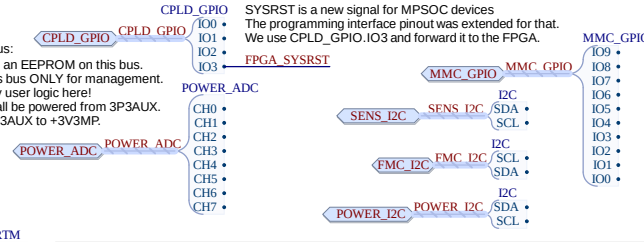


DEBUG Enable - optional

Using this jumper, the MMC Stamp can be taken out of the reset independent of the MCH.
(On-bench-debug for use with SDK)



SYSRST is a new signal for MPSOC devices
The programming interface pinout was extended for that.
We use CPLD_GPIO.IO3 and forward it to the FPGA.



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Project Title: **MTCA_AMC-Template.PrjPcb**
Schematic Title: **DMMC-STAMP SoM**
DATE: 23.01.2025 22:56:08

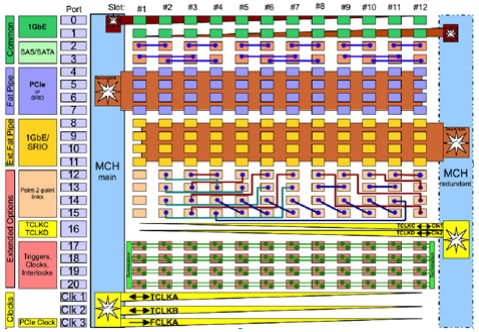
Engineer 1: Michael Fenner
Engineer 2: Robert Wedel

Rev: 0.8
Size: A3
Sheet: 2 of 4

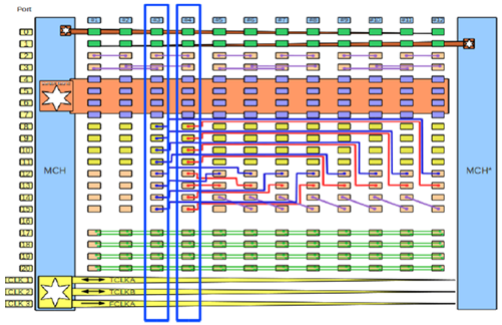
FILENAME: MMC_Stamp.SchDoc

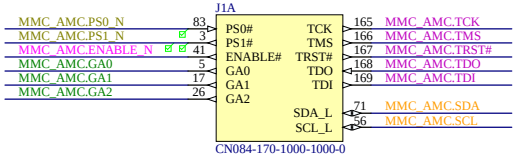
Backplane Connector

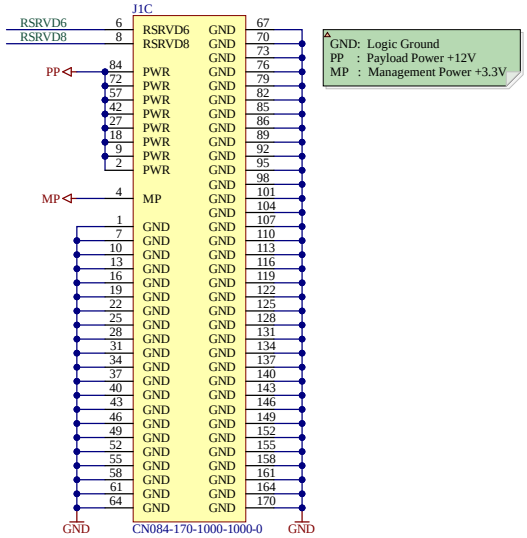
Dual-Star Backplane ("Standard")



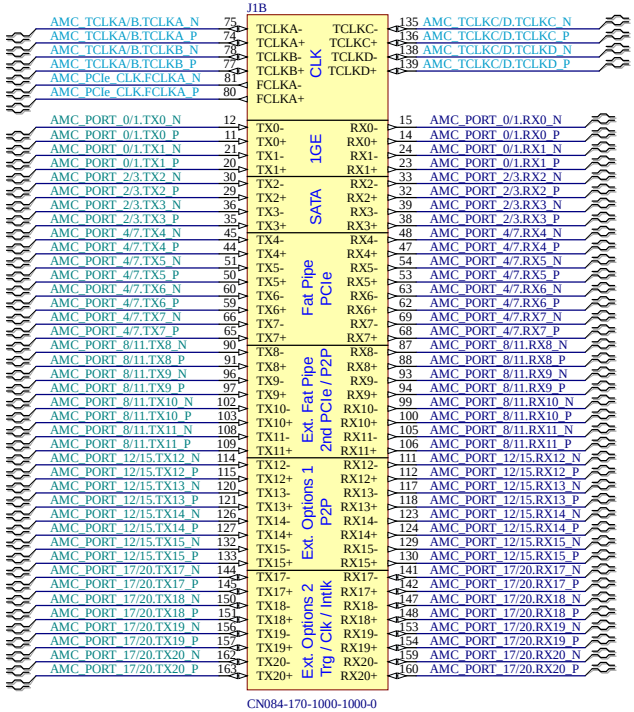
Data aggregation backplane (Introduced by DESY)





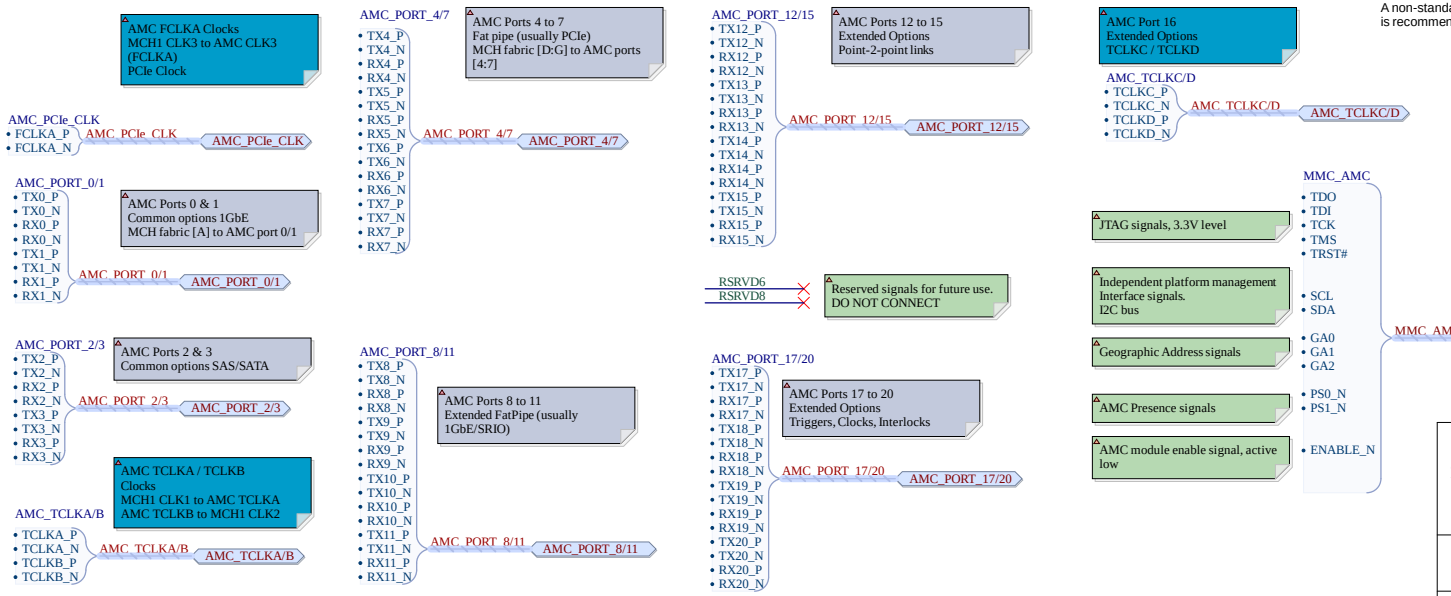


GND: Logic Ground
PP : Payload Power +12V
MP : Management Power +3.3V



DESY uses a backplane connector made by Yamaichi®.
This connector provides perfect mating, less strict requirements for board thickness and usually lower wear of the connectors on the backplane. Compared to a through-hole connector, it has a lower impact on signal integrity.
Data rates of 10Gbps are common to use and show good eye diagrams.
This connector has identical delays for P and N pins. Pay attention to precise P/N manching and FPGA package pin lentgh compensation (flight time matching).

A non-standard footprint is used here. This footprint has optimized signal integrity but is different from what is recommended by the component manufacturer.



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Project Title:
MTCA_AMC-Template.PrjPcb
Schematic Title:
AMC connector
DATE: 23.01.2025 22:56:08

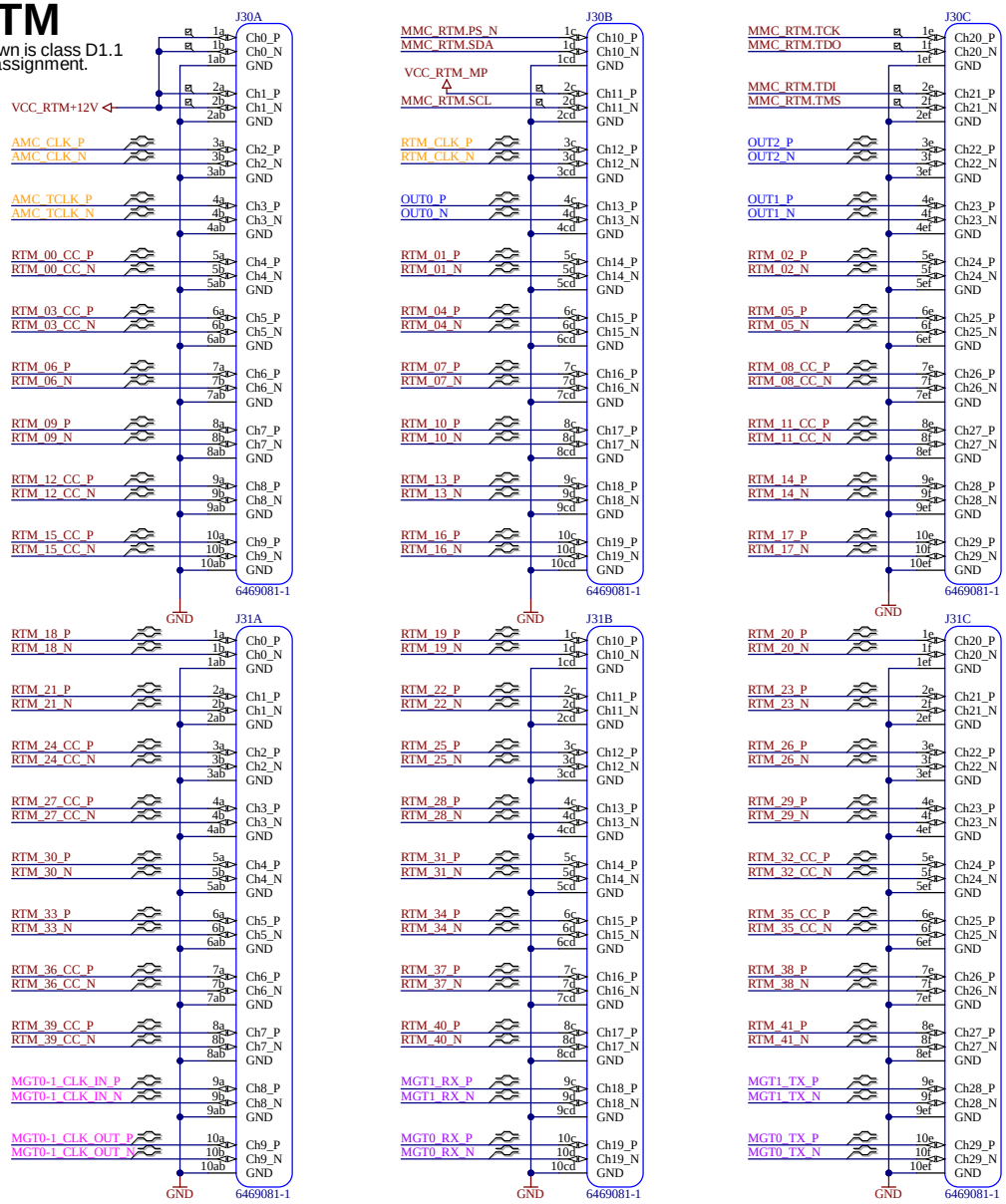
Engineer 1: Robert Wedel
Engineer 2: Michael Fenner

Rev: 0.8
Size: A3
Sheet: 3 of 4

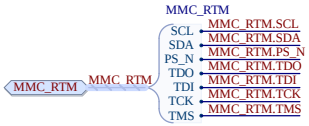
FILENAME: AMC_Z1_connector_basic_side.SchDoc

RTM

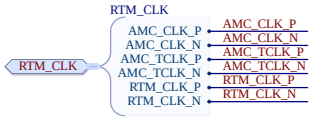
Shown is class D1.1 pin assignment.



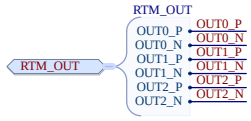
RTM Management



RTM Clocks



RTM Interlocks



Typical assignment on D1.x DESY boards:
All the signals are to be connected to MMC Stamp. JTAG signal level is 3.3V. TDI, TMS, TCK are are AMC outputs going the RTM. TDO is an input on the AMC (output of the RTM). PS_N signals RTM presence (Pull-up inside DMMC-STAMP).

Typical assignment on D1.x DESY boards:
AMC Clock is a clock generated by the clock tree of the AMC. AMC TCLK is a clock that is forwarded from the AMC connector to the RTM (e.g. by using a multiplexer to select between TCLKA or TCLKB). RTM_CLK is a clock output of the RTM, going to the FPGA or Clock tree of the AMC.

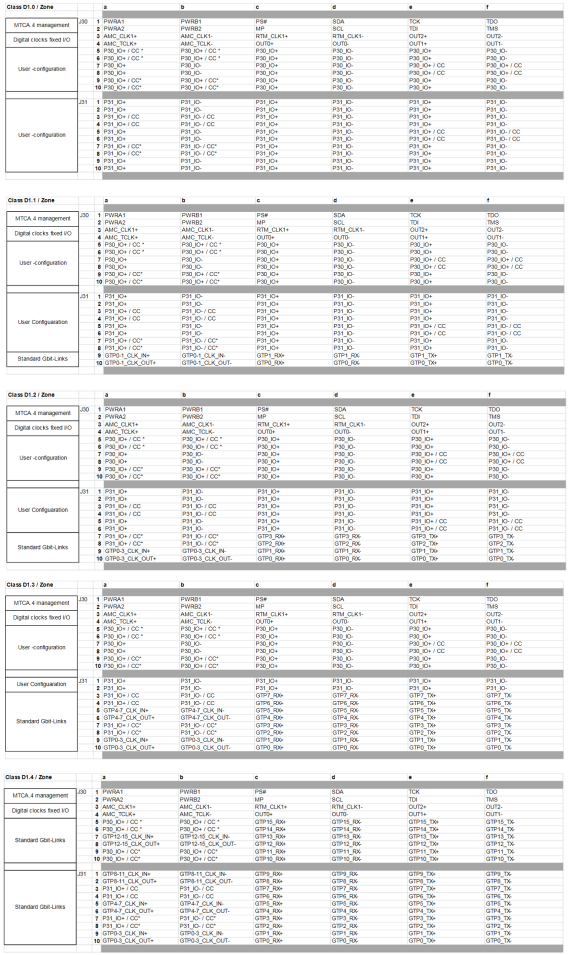
Typical assignment on D1.x DESY boards:
OUT0-2 are fast Interlock signals with LVDS levels. These signals are directly forwarded trigger signals derived from AMC backplane R19_RX, TX19_RX and RX20_RX signals. Signal selection is done via MMC Stamp CLI. Forwarding is done by a CPLD on the MMC Stamp, independent of the user FPGA state.

Typical assignment on D1.x DESY boards:
Usually all RX/TX pins have AC coupling capacitors on the AMC. RX is connected to FPGA MGT RX pin, TX is connected to FPGA MGT TX pin. CLK_IN is a clock output of the RTM, usually going to FPGA MGT reference clock input. CLK_OUT is usually generated by AMC clock tree and synchronous to the MGT reference clock which is used for driving the Zone 3 MGTs.

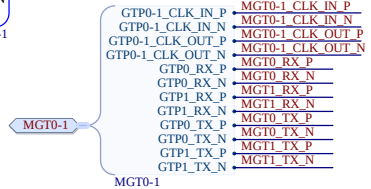
DESY has published Zone 3 pinouts for analog, digital and RF applications:

https://innovation.desy.de/technologies/microtca/support/index_eng.html
- Class D1.0 - D1.4
- Class A1
- Class A2
- Class RF1

Zone 3 Connector Pin Assignment Recommendation for Digital Applications for AMC/µRTM Boards in the MTCA.4 standard (excerpt)



RTM high-speed serial links (MGTs)



LVDS Interface

For information see RTM implementation proposal.

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Project Title: **MTCA_AMC-Template.PrjPcb**
Schematic Title: **RTM Zone 3**
DATE: 23.01.2025 22:56:09

Engineer 1: Robert Wedel
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Rev: 0.8
Size: A3
Sheet: 4 of 4

FILENAME: DRTM_Zone3_D11.SchDoc