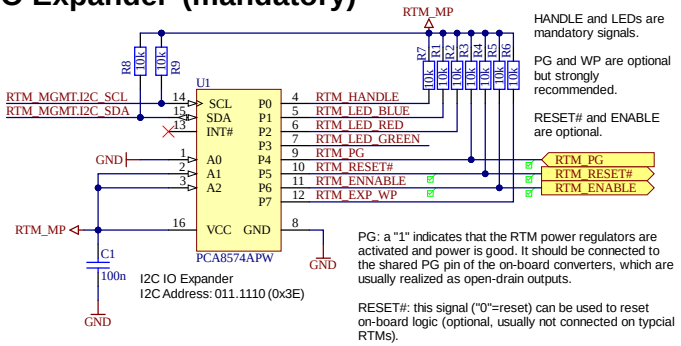
DESY MicroTCA™.4 / 4.1 RTM Implementation Proposal

Draft

IO Expander (mandatory)



HANDLE and LEDs are mandatory signals.

PG and WP are optional but strongly recommended.

RESET# and ENABLE are optional.

PG: a "1" indicates that the RTM power regulators are activated and power is good. It should be connected to the shared PG pin of the on-board converters, which are usually realized as open-drain outputs.

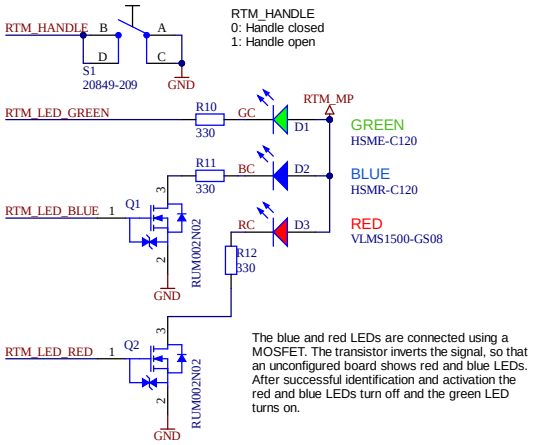
RESET#: this signal ("0"=reset) can be used to reset on-board logic (optional, usually not connected on typcial RTMs).

ENABLE: this signal is used to tristate the Zone 3 interface. "1" means normal operation, "0" means tri-stated interface (optional, usually not connected on typical RTMs).

WP: this signal should be connected to FRU EEPROM WP pin to prevent data corruption during power cycles.

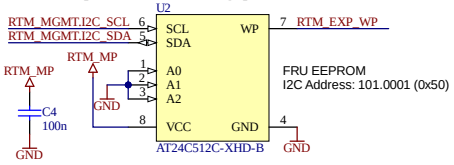
PCA8574A has integrated weak pull-up resistors that source 100uA from VCC. For unused pins, the internal pull-ups usually suffice so that external pull-ups may not be needed.

Handle and LEDs (mandatory)

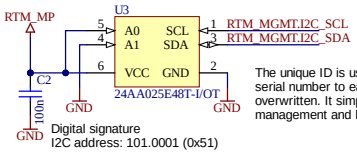


The blue and red LEDs are connected using a MOSFET. The transistor inverts the signal, so that an unconfigured board shows red and blue LEDs. After successful identification and activation the red and blue LEDs turn off and the green LED turns on.

FRU (mandatory)

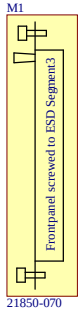


Unique ID (recommneded)

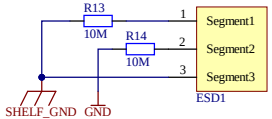


The unique ID is used to assign an individual serial number to each board that can not be overwritten. It simplifies inventory management and board identification.

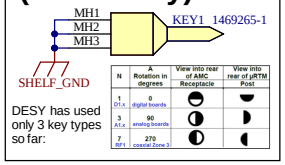
Rear panel (mandatory)



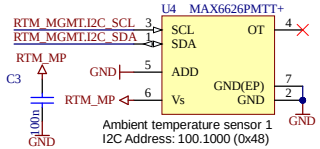
ESD segment (mandatory)



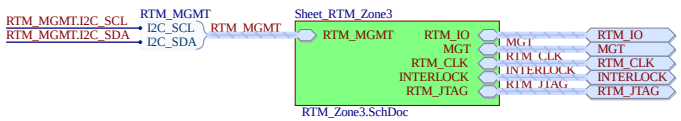
Mechanical key (mandatory)



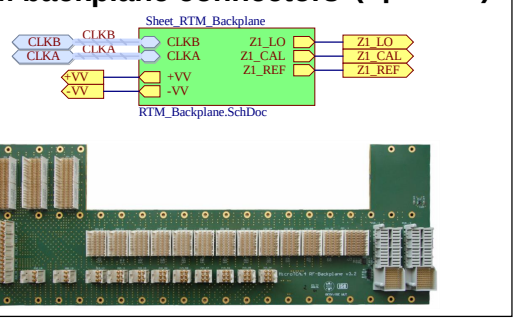
Temperature sensor (recommended)



Zone 3 Connector (mandatory)



RTM backplane connectors (optional)



Single-ended IO support (avoid, if possible)

Information

This is an example RTM implementation proposal. By publishing recommendations, DESY seeks compatibiliy of RTMs to different AMCs. The DESY MMC managment solution is intended to be compatible to this recommendation.

However, AMCs can require vendor-specific management solutions on the RTM, including requirement of different ICs, I2C addresses or special compatiblity records in the FRU.

Always consult the AMC designer for specific RTM implementation reqirements.

Always cross-check with the MicroTCA standard. If in doubt, higher priority shall be given to the standard.

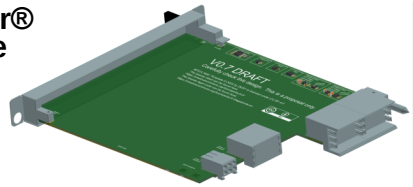
The user is responsible to verify that all implementation details fit to his design requirements.

Disclaimers apply for warranties and limitation of liability. Please check the license terms for more information.

License

Altium Designer® Board Template

The schematics and PCB design files are provided free-of-charge. Please contact DESY.



Fiducials (recommended)

Change List

V0.1 - initial revision
V0.2 - added table of used mechanical keys; changed license text
V0.3 - added change list; added notice on license terms
V0.4 - corrected PG and ENABLE signals to match MTCA.4 standard (had inverted logic in draft MTCA standard)
V0.5 - license set to "TBD".
V0.6 - updated license text (also on PCB)
V0.7pre - update URLs of Z3 Class definitions; add "4.1" wording, add Zone 2 overlay text; remove 3D models; apply CC BY license.
V0.7 - add CC-license compatible 3D modes to all parts.

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Project Title:
RTM-Template.PrjPcb
Schematic Title:
RTM Managment Top
DATE: 06.02.2024 20:14:58

Engineer 1: Michael Fenner
Engineer 2: Robert Wedel

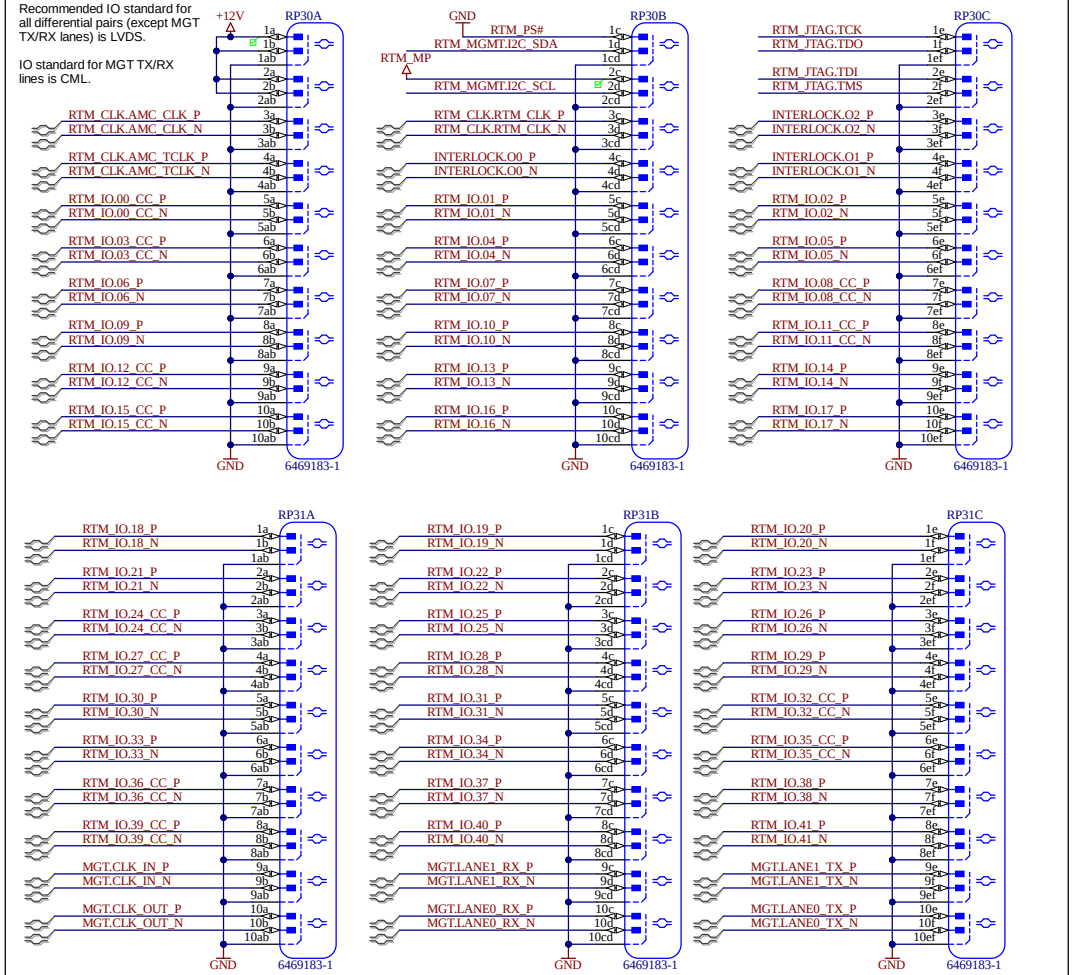
Rev: 0.7
Size: A3
Sheet: 1 of 4

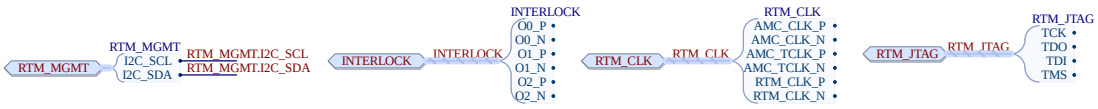
FILENAME: DRTM-Template_TOP.SchDoc

Zone 3

Recommended IO standard for all differential pairs (except MGT TX/RX lanes) is LVDS.

IO standard for MGT TX/RX lines is CML.





Management I2C (mandatory and standardized)
The MTCA standard requires the connection an I2C expander for hot-swap handle, LEDs and control signals on address 0x3E. The pin assignment is precisely defined. A FRU EEPROM is expected on address 0x50. In addition, DESY recommends an unique ID chip on address 0x51 for board identification and a MAX6626 temperature sensor on address 0x48.

Interlock (optional and vendor-specific)
The interlock lines allow implementation of machine safety functions on the RTM (e.g. fast power switch-off).
DESY MMC implementation: The MMC forwards AMC backplane MLVDS signals to the RTM. This interface is driven by a CPLD (backplane assignment depends on user setting), allowing reliable operation independent of the AMC FPGA status. IO standard is LVDS.

RTM clocks (optional and vendor-specific)
The clock lines allows AMC and RTM to exchange reference clocks.
DESY Implementation: AMC_CLK is a signal generated by the clock generator on AMC (typically a PLL). RTM_CLK is signal generated by the RTM (usually a PLL or the output of an ADC). AMC_TCLK is typically driven by a multiplexer, allowing to forward TCLKA or TCLKB from the AMC backplane to the RTM. IO standard is LVDS.

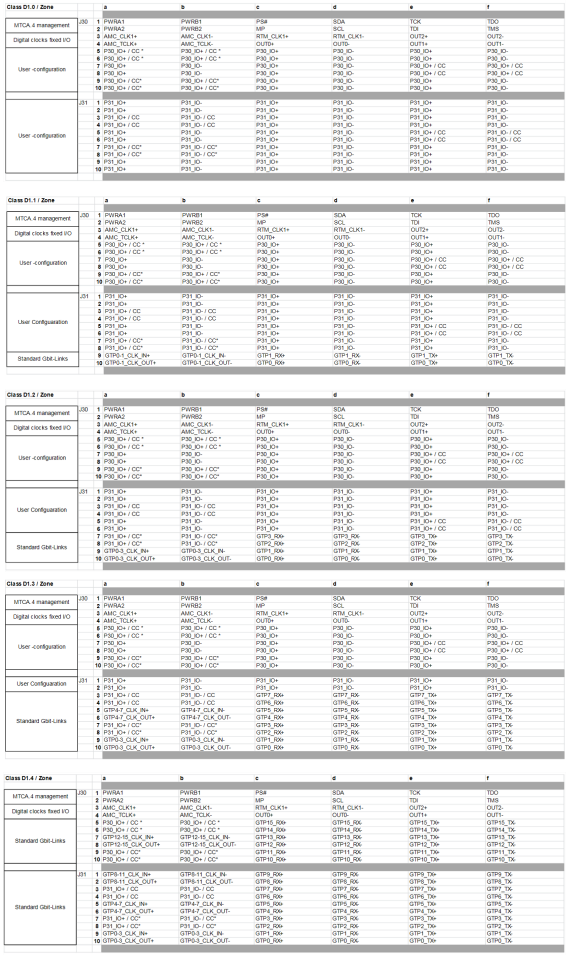
JTAG (optional and vendor-specific)
This interface allows remote programming and debugging of the RTM (e.g. via virtual JTAG probe in MCH).
DESY MMC implementation:
Depending on user configuration, AMC on-board JTAG connector signals or main backplane JTAG signals are forwarded to these pins.TDI is an input into the RTM, TDO is an output of the RTM (1-to-1 connection of FPGA on RTM, no TDI/TDO swapping). IO

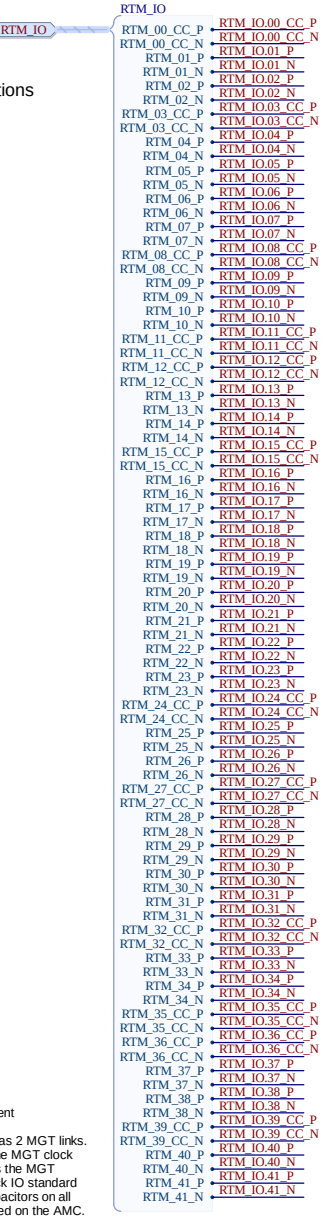
DESY has published Zone 3 pinouts for analog, digital and RF applications:

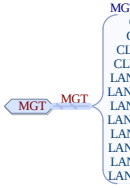
https://innovation.desy.de/technologies/microtca/support/index_eng.html

Class D1.0 - D1.4
Class A1 Class A2
Class RF1

Zone 3 Connector Pin Assignment Recommendation for Digital Applications for AMC/µRTM Boards in the MTCA.4 standard (excerpt)







MGT connection (optional and defined by DESY Zone 3 connector pin assignment recommendation)
The number of MGTs is dependent on the chosen interface class. Class D1.1 has 2 MGT links.
CLK_OUT is an output of the AMC (driven by AMC) and usually derived from the MGT clock generator. CLK_IN is an output of the RTM (driven by RTM) that usually carries the MGT reference clock for direct connection to FPGA MGT bank (MGT_REFCLK). Clock IO standard is LVDS. MGT IO standard is CML. Modern DESY boards have AC coupling capacitors on all MGT TX and RX lines. The CLK_OUT input (AMC to RTM) is usually DC-coupled on the AMC. The clock output (RTM to AMC) is usually AC coupled on the AMC (FPGA requirement for MGT reference clocks)
TX means output of AMC (AMC to RTM). RX means input of AMC (RTM to AMC).

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Project Title:
RTM-Template.PrjPcb
Schematic Title:
Zone 3 Connector
DATE: 06.02.2024 20:14:58

Engineer 1: Robert Wedel
Engineer 2: Michael Fenner

Rev: 0.7
Size: A3
Sheet: 2 of 4

FILENAME: RTM_Zone3.SchDoc

Single-Ended IOs (optional)

Do I need single-ended IOs on Zone 3? (not recommended)

no — **perfect!**

yes — **recommended implementation**

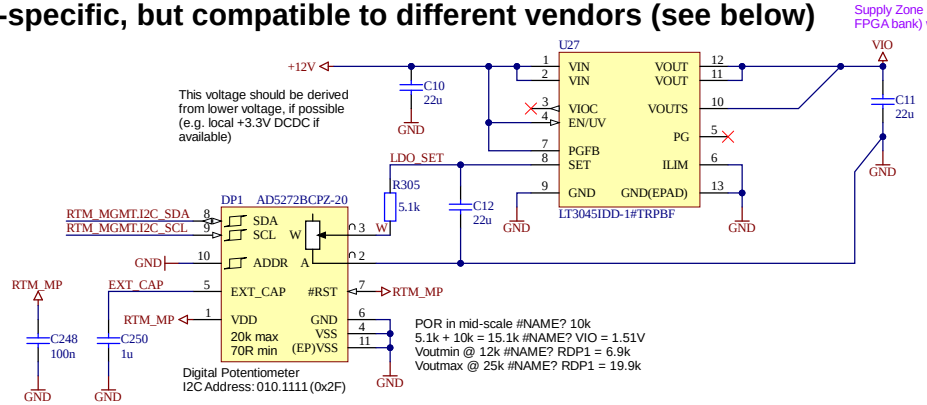
yes — **DESY boards only legacy implementation**

LVDS only - no single ended IOs (recommended)

No extra components needed, ignore this page!

DESY recommends to use only LVDS signals on all RTM-IO pins. LVDS is a common standard and will always be compatible, independent of FPGA bank IO voltage. By using LVDS signals only, no glue logic, no voltage translation and no coupling capacitors are necessary. Translating single-ended interfaces (such as SPI) to LVDS to cross Zone 3 is preferred and requires no variable voltage supply or interaction with MMC management. However, there are cases (e.g. where more signals need to be transferred over Zone 3 than pins are available) where the user decides to use single-ended IOs. In this case, a variable IO voltage on all these these signals is needed. Depending which FPGA type and which bank voltage was chosen on the AMC, the voltage of the Zone 3 has to be configured to precisely to match the FPGA bank voltage. Failing to adhere to the specific bank voltage requirement will exceed the abolute maximum ratings, may damage the AMC and will not work, in any case. A circuit for the bank voltage setting is highly proprietary and has to be specifically supported by the module management controller (MMC) on the AMC. The following implementations are supported by DESY MMC. Single-ended RTM IOs shall be avoided wherever possible.

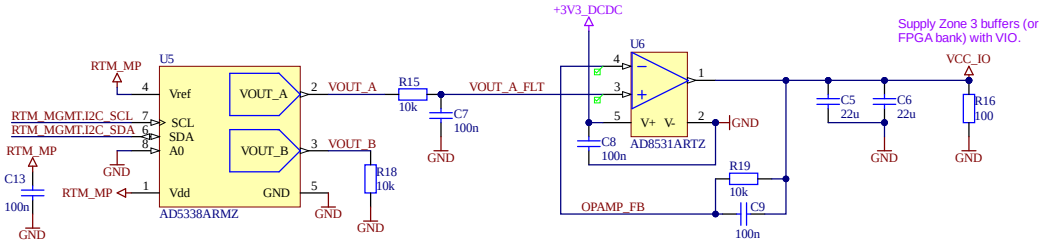
Single-ended IO voltage generation with LDO
DESY-specific, but compatible to different vendors (see below)



Depending on the chosen FPGA bank voltage on AMC, a matching Zone 3 voltage has to be selected. Old FPGAs (Virtex®-4, Virtex®-5 support bank voltages of up to 3.3V. Most DESY boards used 2.5V bank voltage on the Zone3 interface. Modern FPGAs (Ultrascale® and newer) mostly support 1.8V on Zone 3 only. If single-ended IOs on Zone 3 are needed, DESY recommends this circuit. The MMC on the AMC will set up the digital potentiometer in such a way that LDO generates the IO voltage that matches the specific FPGA bank voltage. It is supported by DESY MMC Stamp and support will be added to the MMC of older DESY designs such as DAMC-FMC25, DAMC-FMC20 and DAMC-TCK7.

The digital potentiometer can be programmed to a fixed start-up value (non-volatile memory). Support of one specific 3rd-party AMC board can be achieved by programming a fixed value into the resistor, resulting in a correct (but fixed) Zone 3 voltage. If the AMC board is changed, the potentiometer may have to be re-programmed with a different value. This solution is, even if it is proprietary, the most flexible way to allow single-ended IO compatiblity accross multiple vendors and MMC solutions, respectively.

Single-Ended IO voltage generation with DAC (legacy, not recommended)



This is the solution is used on all legacy DESY RTMs (DRTM-AD84, DRTM-PZT4, DRTM-DWC10, DRTM-DWC8VM1, etc.). It is also supported by Struck SIS8300L2 and SIS8325 and SIS8300KU. This concept uses a DAC that is controlled by the MMC on the AMC. The disadvantage of the solution is that it only supports currents up to 250mA, it needs external voltage (+3V3_DCDC here) and the AMC has to be aware of this solution and has to specifically support it. 3rd-party AMCs that are not adapted to this solution, can not operate the RTM at all. However, all existing AMCs with DESY MMC V1.00 or DESY MMC Stamp will support this solution out-of-the-box.

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Project Title: **RTM-Template.PrjPcb**
Schematic Title: **Zone 3 single-ended IO**
DATE: 06.02.2024 20:14:59

Engineer 1: Michael Fenner
Engineer 2: Johannes Zink

FILENAME: RTM_Single_Ended_IO.SchDoc

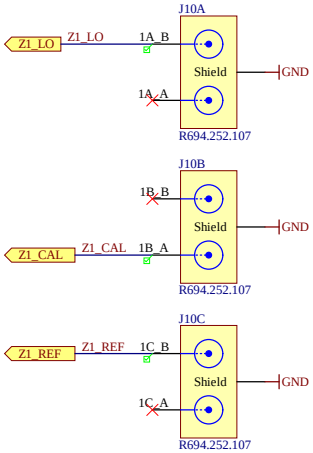
Rev: 0.7
Size: A3
Sheet: 3 of 4

RTM Backplane Connectors (optional)

The MicroTCA specification Revision 4.1 defines an optional RTM backplane. It is used for distribution of high-precision clocks inside the chassis to MicroTCA RTMs. In addition, a clean bipolar supply voltage can be distributed on this backplane. Special eRTMs (without connection to AMC backplane) generate precision clocks and reference signals for the RTMs. A special rear power module can generate a clean supply voltage for the RTMs. Management of the eRTMs and rear power supplies is realised by using a MCH-RTM, which forwards the rear managment signals the front MCH.

A 12-slot chassis with the shown RTM backplane is available from nVent / Schroff GmbH. A modular rear power module and the MCH-RTM are available from N.A.T. GmbH. The DRTM-LOG1300 is available from DESY.

RTM Backplane Zone 1
RF cock input



connetor pinout for slots #4-#12

	A	B
1A	rfu	LO
1B	CAL	rfu
1C	rfu	REF

rfu – pins reserved for future use

RF_CONF Settings

The voltage on RF_CONF is used to request a specific clock assignment on the Zone1 and Zone 2 connectors. A fixed voltage coming from a simple resistor divider can be presented here. Alternatively the voltage can be generated using an electronic potentiometer for maximum flexibility. (5V supply is required for full scale setting.)

Table 3: RF_CONF signal voltage levels and their assignment

State	CLKs LO CAL REF [1=yes, 0=no]	Required DC level [V]	Lower limit [V]	Upper limit [V]
1	0000	0,4	0,26	0,54
2	0001	0,68	0,54	0,82
3	0010	0,96	0,82	1,1
4	0011	1,24	1,1	1,38
5	0100	1,52	1,38	1,66
6	0101	1,8	1,66	1,94
7	0110	2,08	1,94	2,22
8	0111	2,36	2,22	2,5
9	1000	2,64	2,5	2,78
10	1001	2,92	2,78	3,06
11	1010	3,2	3,06	3,34
12	1011	3,48	3,34	3,62
13	1100	3,76	3,62	3,9
14	1101	4,04	3,9	4,18
15	1110	4,32	4,18	4,46
16	1111	4,6	4,46	4,74

RTM Backplane Zone 2
Analog voltage and additional clocks

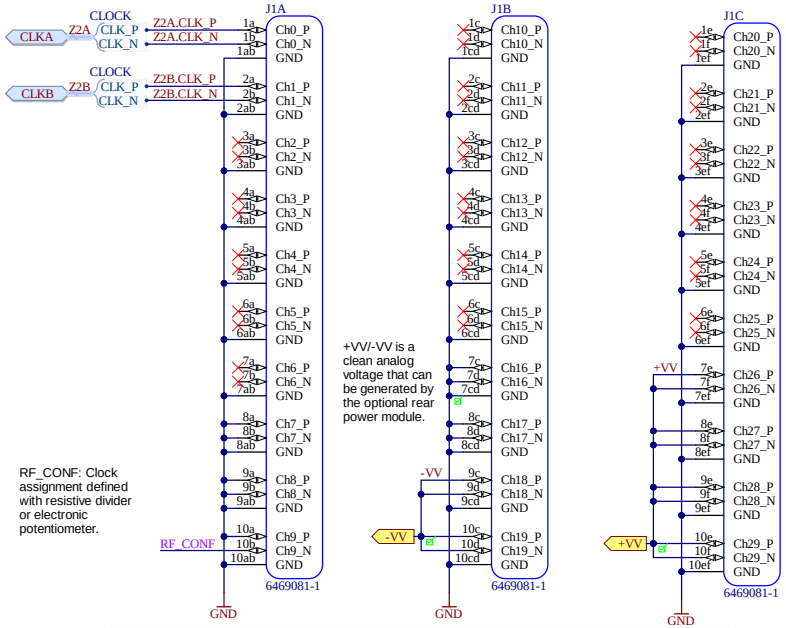
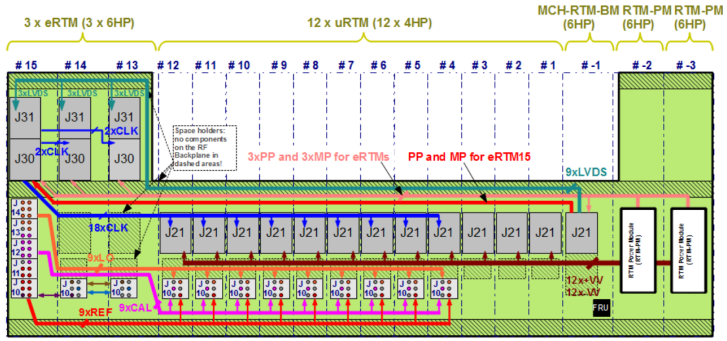


Table 20: J21 connetor pinout for slots #4+#12

	a	b	ab	c	d	cd	e	f	ef
1	CLKxA_P	CLKxA_N	GND	rfu	rfu	GND	rfu	rfu	GND
2	CLKxB_P	CLKxB_N	GND	rfu	rfu	GND	rfu	rfu	GND
3	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
4	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
5	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
6	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
7	rfu	rfu	GND	GND	GND	GND	+VV	+VV	GND
8	GND	GND	GND	GND	GND	GND	+VV	+VV	GND
9	GND	GND	GND	-VV	-VV	GND	+VV	+VV	GND
10	PS1#	RF_CONF	GND	-VV	-VV	GND	+VV	+VV	GND

rfu – pins reserved for future use

Connectivity of DESY RTM Backplane



DRTM-LOG1300 - eRTM clock generator

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Project Title: **RTM-Template.PrjPcb**
Schematic Title: **RTM Backplane Connectors**
DATE: 06.02.2024 20:14:59

Engineer 1: Michael Fenner
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FILENAME: RTM_Backplane.SchDoc

Rev: 0.7
Size: A3
Sheet: 4 of 4