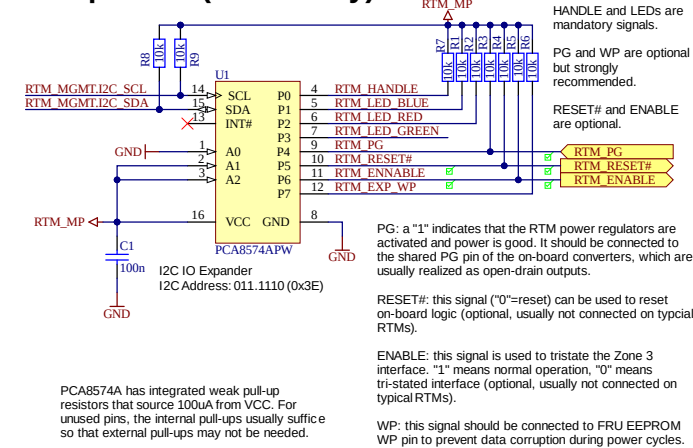


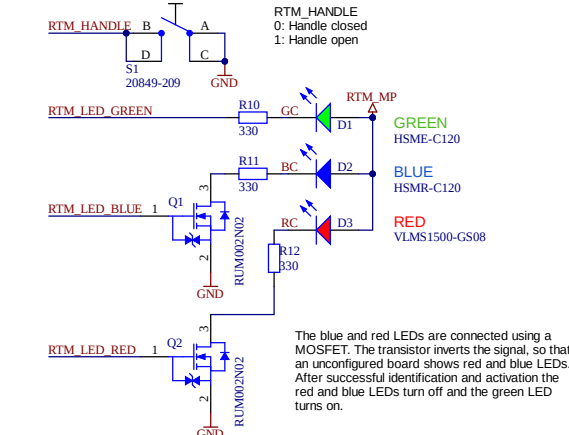
DESY MicroTCA™.4 / 4.1 RTM Implementation Proposal

Draft

IO Expander (mandatory)



Handle and LEDs (mandatory)



Information

This is an example RTM implementation proposal. By publishing recommendations, DESY seeks compatibility of RTMs to different AMCs. The DESY MMC management solution is intended to be compatible to this recommendation.

However, AMCs may require vendor-specific management solutions on the RTM, including requirement of different ICs, I2C addresses or special compatibility records in the FRU.

Always consult the AMC designer for specific RTM implementation requirements.

Always cross-check with the MicroTCA standard. If in doubt, higher priority shall be given to the standard.

The user is responsible to verify that all implementation details fit to his design requirements.

Disclaimers apply for warranties and limitation of liability. Please check the license terms for more information.

License

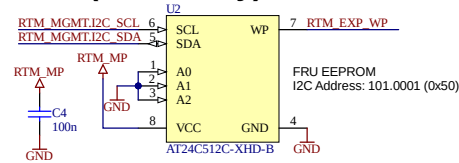
MTCA AMC Template © 2024 by DESY is licensed under CC BY 4.0

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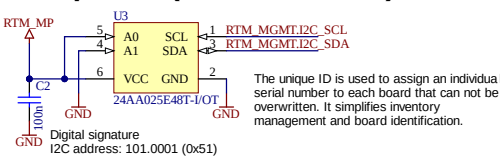
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FRU (mandatory)



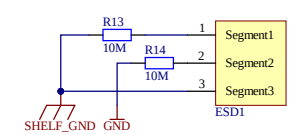
Unique ID (recommended)



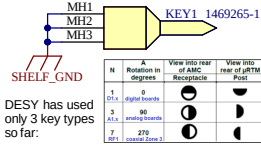
Rear panel (mandatory)



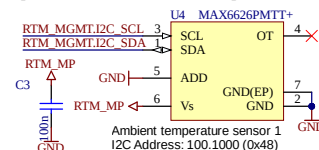
ESD segment (mandatory)



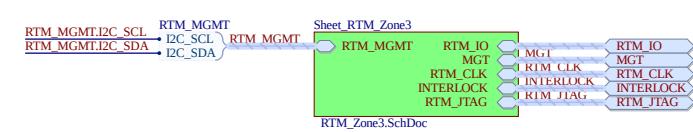
Mechanical key (mandatory)



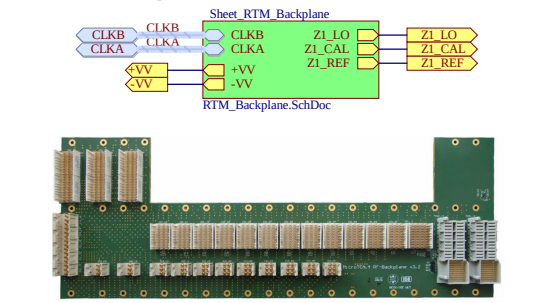
Temperature sensor (recommended)



Zone 3 Connector (mandatory)



RTM backplane connectors (optional)

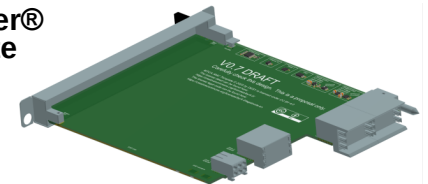


Single-ended IO support (avoid, if possible)



Altium Designer® Board Template

The schematics and PCB design files are provided free-of-charge. Please contact DESY.



Fiducials (recommended)



Change List

- V0.1 - initial revision
- V0.2 - added table of used mechanical keys; changed license text
- V0.3 - added change list; added notice on license terms
- V0.4 - corrected PG and ENABLE signals to match MTCA.4 standard (had inverted logic in draft MTCA standard)
- V0.5 - license set to "BY"
- V0.6 - updated license text (also on PCB)
- V0.7pre - update URLs of Z3 Class definitions; add "4.1" wording; add Zone 2 overlay text; remove 3D models; apply CC BY license.
- V0.7 - add CC-license compatible 3D models to all parts.



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FILENAME: DRTM-Template_TOP.SchDoc

Project Title:
RTM-Template.PrjPcb
Schematic Title:
RTM Management Top
DATE: 06.02.2024 20:14:58

Engineer 1: Michael Fenner
Engineer 2: Robert Wedel



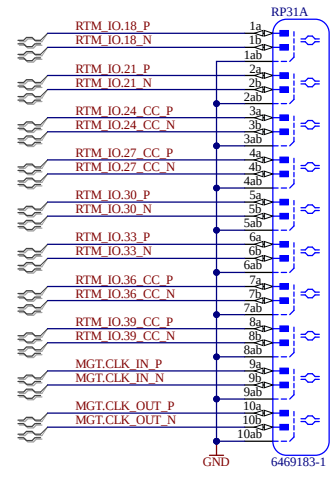
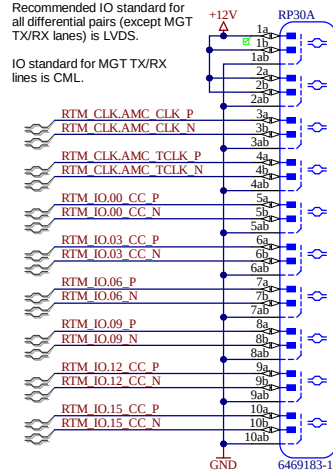
Rev: 0.7
Size: A3
Sheet:

1 of 4

Zone 3

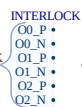
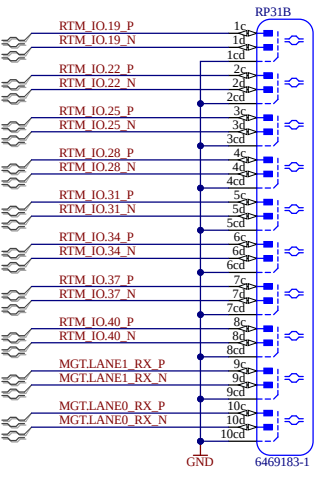
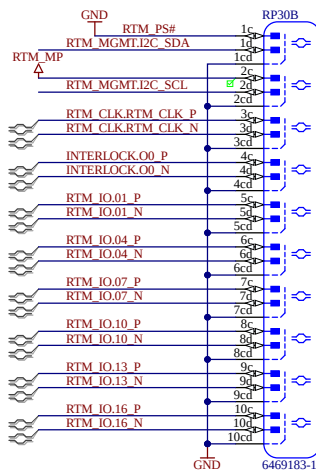
Recommended IO standard for all differential pairs (except MGT TX/RX lanes) is LVDS.

IO standard for MGT TX/RX lines is CML.

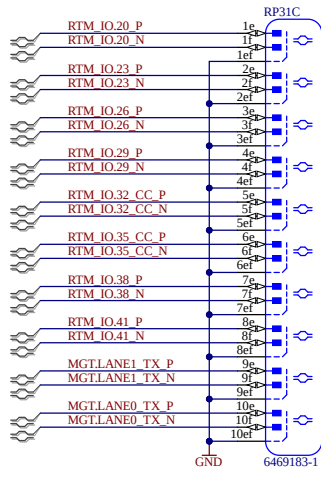
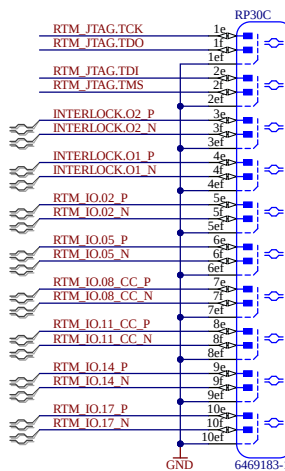


Management I2C (mandatory and standardized)
The MTCA standard requires the connection an I2C expander for hot-swap handle, LEDs and control signals on address 0x3E. The pin assignment is precisely defined. A FRU EEPROM is expected on address 0x50. In addition, DESY recommends a unique ID chip on address 0x51 for board identification and a MAX6626 temperature sensor on address 0x48.

Interlock (optional and vendor-specific)
The interlock lines allow implementation of machine safety functions on the RTM (e.g. fast power switch-off).
DESY MMC implementation: The MMC forwards AMC backplane MLVDS signals to the RTM. This interface is driven by a CPLD (backplane assignment depends on user setting), allowing reliable operation independent of the AMC FPGA status. IO standard is LVDS.



RTM clocks (optional and vendor-specific)
The clock lines allows AMC and RTM to exchange reference clocks.
DESY Implementation: AMC_CLK is a signal generated by the clock generator on AMC (typically a PLL). RTM_CLK is signal generated by the RTM (usually a PLL or the output of an ADC). AMC_TCLK is typically driven by a multiplexer, allowing to forward TCLKA or TCLKB from the AMC backplane to the RTM. IO standard is LVDS.



JTAG (optional and vendor-specific)
This interface allows remote programming and debugging of the RTM (e.g. via virtual JTAG probe in MCH).

DES9 MMC implementation:
Depending on user configuration, AMC on-board JTAG connector signals or main backplane JTAG signals are forwarded to these pins. TDI is an input into the RTM, TDO is an output of the RTM (1-to-1 connection of FPGA on RTM, no TDI/TDO swapping). IO

DESY has published Zone 3 pinouts for analog, digital and RF applications:

https://innovation.desy.de/technologies/microtca/support/index_eng.html
 Class D1.0 - D1.4
 Class A1 Class A2
 Class RF1

Zone 3 Connector Pin Assignment Recommendation for Digital Applications for AMC/ μ RTM Boards in the MTCA.4 standard (excerpt)

Clock ID & Name		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
MPIC & management	1	PM0A1	PM0B1	PM0C1	PM0D1	PM0E1	PM0F1	PM0G1	PM0H1	PM0I1	PM0J1	PM0K1	PM0L1	PM0M1	PM0N1	PM0O1	PM0P1	PM0Q1	PM0R1	PM0S1	PM0T1	PM0U1	PM0V1	PM0W1	PM0X1	PM0Y1	PM0Z1
	2	PM0A2	PM0B2	PM0C2	PM0D2	PM0E2	PM0F2	PM0G2	PM0H2	PM0I2	PM0J2	PM0K2	PM0L2	PM0M2	PM0N2	PM0O2	PM0P2	PM0Q2	PM0R2	PM0S2	PM0T2	PM0U2	PM0V2	PM0W2	PM0X2	PM0Y2	PM0Z2
Digital clocks based IO	3	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1	AMC_CLK1
	4	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2	AMC_CLK2
User configuration	5	PM0A1+CC	PM0B1+CC	PM0C1+CC	PM0D1+CC	PM0E1+CC	PM0F1+CC	PM0G1+CC	PM0H1+CC	PM0I1+CC	PM0J1+CC	PM0K1+CC	PM0L1+CC	PM0M1+CC	PM0N1+CC	PM0O1+CC	PM0P1+CC	PM0Q1+CC	PM0R1+CC	PM0S1+CC	PM0T1+CC	PM0U1+CC	PM0V1+CC	PM0W1+CC	PM0X1+CC	PM0Y1+CC	PM0Z1+CC
	6	PM0A1+CC	PM0B1+CC	PM0C1+CC	PM0D1+CC	PM0E1+CC	PM0F1+CC	PM0G1+CC	PM0H1+CC	PM0I1+CC	PM0J1+CC	PM0K1+CC	PM0L1+CC	PM0M1+CC	PM0N1+CC	PM0O1+CC	PM0P1+CC	PM0Q1+CC	PM0R1+CC	PM0S1+CC	PM0T1+CC	PM0U1+CC	PM0V1+CC	PM0W1+CC	PM0X1+CC	PM0Y1+CC	PM0Z1+CC
User configuration	7	PM0A1+CC	PM0B1+CC	PM0C1+CC	PM0D1+CC	PM0E1+CC	PM0F1+CC	PM0G1+CC	PM0H1+CC	PM0I1+CC	PM0J1+CC	PM0K1+CC	PM0L1+CC	PM0M1+CC	PM0N1+CC	PM0O1+CC	PM0P1+CC	PM0Q1+CC	PM0R1+CC	PM0S1+CC	PM0T1+CC	PM0U1+CC	PM0V1+CC	PM0W1+CC	PM0X1+CC	PM0Y1+CC	PM0Z1+CC
	8	PM0A1+CC	PM0B1+CC	PM0C1+CC	PM0D1+CC	PM0E1+CC	PM0F1+CC	PM0G1+CC	PM0H1+CC	PM0I1+CC	PM0J1+CC	PM0K1+CC	PM0L1+CC	PM0M1+CC	PM0N1+CC	PM0O1+CC	PM0P1+CC	PM0Q1+CC	PM0R1+CC	PM0S1+CC	PM0T1+CC	PM0U1+CC	PM0V1+CC	PM0W1+CC	PM0X1+CC	PM0Y1+CC	PM0Z1+CC

[illegible]

Clock ID / Zone		A	B	C	D	E	F
MPIC / management	200	PW001	PW002	P00	P00	P00	P00
	201	PW001	PW002	P00	P00	P00	P00
Digital clocks beat ID	202	AMC_CLK_0	AMC_CLK_1	BTCL_CLK_0	BTCL_CLK_1	OUT_0	OUT_1
	203	AMC_CLK_0	AMC_CLK_1	OUT_0	OUT_1	OUT_0	OUT_1
User configuration	204	P00_0_0	P00_0_0	P00_0_0	P00_0_0	P00_0_0	P00_0_0
	205	P00_0_0	P00_0_0	P00_0_0	P00_0_0	P00_0_0	P00_0_0
User Configuration	206	P00_0_0	P00_0_0	P00_0_0	P00_0_0	P00_0_0	P00_0_0
	207	P00_0_0	P00_0_0	P00_0_0	P00_0_0	P00_0_0	P00_0_0
Standard GEM-Lets	208	GEM0_CLK_0	GEM0_CLK_1	GEM1_CLK_0	GEM1_CLK_1	GEM2_CLK_0	GEM2_CLK_1
	209	GEM0_CLK_0	GEM0_CLK_1	GEM1_CLK_0	GEM1_CLK_1	GEM2_CLK_0	GEM2_CLK_1

Status D1.3 / Zone						
OTIS A management	1	P000A1	P000B1	P000C1	P000D1	P000E1
OTIS B management	2	P000B1	P000B1	P000B1	P000B1	P000B1
Digital clocks feed IO	3	AMC-TCL-A	AMC-TCL-B	AMC-TCL-C	AMC-TCL-D	AMC-TCL-E
User configuration	4	P001-C1-CC	P001-C1-CC	P001-C1-CC	P001-C1-CC	P001-C1-CC
	5	P001-C1-CC	P001-C1-CC	P001-C1-CC	P001-C1-CC	P001-C1-CC
	6	P001-C1-CC	P001-C1-CC	P001-C1-CC	P001-C1-CC	P001-C1-CC
	7	P001-C1-CC	P001-C1-CC	P001-C1-CC	P001-C1-CC	P001-C1-CC
User Configuration	8	P01-C0	P01-C0	P01-C0	P01-C0	P01-C0
	9	P01-C0	P01-C0	P01-C0	P01-C0	P01-C0
	10	P01-C0	P01-C0	P01-C0	P01-C0	P01-C0
	11	P01-C0	P01-C0	P01-C0	P01-C0	P01-C0
Standard test cases	12	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1
	13	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1
	14	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1
	15	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1
	16	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1
	17	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1
	18	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1
	19	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1
	20	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1
	21	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1	G000-C1-Out1

Device D14 / Zone							
MTPLC management	250	P00011	P00011	P00011	P00011	P00011	P00011
		P00012	P00012	P00012	P00012	P00012	P00012
Digital circuits board IO		AMC-CLK+	AMC-CLK-	AMC-CLK+	AMC-CLK-	AMC-CLK+	AMC-CLK-
		PS2-IO+	PS2-IO-	PS2-IO+	PS2-IO-	PS2-IO+	PS2-IO-
Standard GDS-Lines		GDS10-15_CLK_In	GDS10-15_CLK_Out	GDS10-15_CLK_In	GDS10-15_CLK_Out	GDS10-15_CLK_In	GDS10-15_CLK_Out
		GDS10-15_CLK_In	GDS10-15_CLK_Out	GDS10-15_CLK_In	GDS10-15_CLK_Out	GDS10-15_CLK_In	GDS10-15_CLK_Out
Standard GDS-Lines		GDS11-16_CLK_In	GDS11-16_CLK_Out	GDS11-16_CLK_In	GDS11-16_CLK_Out	GDS11-16_CLK_In	GDS11-16_CLK_Out
		GDS11-16_CLK_In	GDS11-16_CLK_Out	GDS11-16_CLK_In	GDS11-16_CLK_Out	GDS11-16_CLK_In	GDS11-16_CLK_Out
Standard GDS-Lines		GDS17-22_CLK_In	GDS17-22_CLK_Out	GDS17-22_CLK_In	GDS17-22_CLK_Out	GDS17-22_CLK_In	GDS17-22_CLK_Out
		GDS17-22_CLK_In	GDS17-22_CLK_Out	GDS17-22_CLK_In	GDS17-22_CLK_Out	GDS17-22_CLK_In	GDS17-22_CLK_Out
Standard GDS-Lines		GDS23-28_CLK_In	GDS23-28_CLK_Out	GDS23-28_CLK_In	GDS23-28_CLK_Out	GDS23-28_CLK_In	GDS23-28_CLK_Out
		GDS23-28_CLK_In	GDS23-28_CLK_Out	GDS23-28_CLK_In	GDS23-28_CLK_Out	GDS23-28_CLK_In	GDS23-28_CLK_Out
Standard GDS-Lines		GDS29-34_CLK_In	GDS29-34_CLK_Out	GDS29-34_CLK_In	GDS29-34_CLK_Out	GDS29-34_CLK_In	GDS29-34_CLK_Out
		GDS29-34_CLK_In	GDS29-34_CLK_Out	GDS29-34_CLK_In	GDS29-34_CLK_Out	GDS29-34_CLK_In	GDS29-34_CLK_Out
Standard GDS-Lines		GDS35-40_CLK_In	GDS35-40_CLK_Out	GDS35-40_CLK_In	GDS35-40_CLK_Out	GDS35-40_CLK_In	GDS35-40_CLK_Out
		GDS35-40_CLK_In	GDS35-40_CLK_Out	GDS35-40_CLK_In	GDS35-40_CLK_Out	GDS35-40_CLK_In	GDS35-40_CLK_Out
Standard GDS-Lines		GDS41-46_CLK_In	GDS41-46_CLK_Out	GDS41-46_CLK_In	GDS41-46_CLK_Out	GDS41-46_CLK_In	GDS41-46_CLK_Out
		GDS41-46_CLK_In	GDS41-46_CLK_Out	GDS41-46_CLK_In	GDS41-46_CLK_Out	GDS41-46_CLK_In	GDS41-46_CLK_Out
Standard GDS-Lines		GDS47-52_CLK_In	GDS47-52_CLK_Out	GDS47-52_CLK_In	GDS47-52_CLK_Out	GDS47-52_CLK_In	GDS47-52_CLK_Out
		GDS47-52_CLK_In	GDS47-52_CLK_Out	GDS47-52_CLK_In	GDS47-52_CLK_Out	GDS47-52_CLK_In	GDS47-52_CLK_Out
Standard GDS-Lines		GDS53-58_CLK_In	GDS53-58_CLK_Out	GDS53-58_CLK_In	GDS53-58_CLK_Out	GDS53-58_CLK_In	GDS53-58_CLK_Out
		GDS53-58_CLK_In	GDS53-58_CLK_Out	GDS53-58_CLK_In	GDS53-58_CLK_Out	GDS53-58_CLK_In	GDS53-58_CLK_Out
Standard GDS-Lines		GDS59-64_CLK_In	GDS59-64_CLK_Out	GDS59-64_CLK_In	GDS59-64_CLK_Out	GDS59-64_CLK_In	GDS59-64_CLK_Out
		GDS59-64_CLK_In	GDS59-64_CLK_Out	GDS59-64_CLK_In	GDS59-64_CLK_Out	GDS59-64_CLK_In	GDS59-64_CLK_Out
Standard GDS-Lines		GDS65-70_CLK_In	GDS65-70_CLK_Out	GDS65-70_CLK_In	GDS65-70_CLK_Out	GDS65-70_CLK_In	GDS65-70_CLK_Out
		GDS65-70_CLK_In	GDS65-70_CLK_Out	GDS65-70_CLK_In	GDS65-70_CLK_Out	GDS65-70_CLK_In	GDS65-70_CLK_Out
Standard GDS-Lines		GDS71-76_CLK_In	GDS71-76_CLK_Out	GDS71-76_CLK_In	GDS71-76_CLK_Out	GDS71-76_CLK_In	GDS71-76_CLK_Out
		GDS71-76_CLK_In	GDS71-76_CLK_Out	GDS71-76_CLK_In	GDS71-76_CLK_Out	GDS71-76_CLK_In	GDS71-76_CLK_Out
Standard GDS-Lines		GDS77-82_CLK_In	GDS77-82_CLK_Out	GDS77-82_CLK_In	GDS77-82_CLK_Out	GDS77-82_CLK_In	GDS77-82_CLK_Out
		GDS77-82_CLK_In	GDS77-82_CLK_Out	GDS77-82_CLK_In	GDS77-82_CLK_Out	GDS77-82_CLK_In	GDS77-82_CLK_Out
Standard GDS-Lines		GDS83-88_CLK_In	GDS83-88_CLK_Out	GDS83-88_CLK_In	GDS83-88_CLK_Out	GDS83-88_CLK_In	GDS83-88_CLK_Out
		GDS83-88_CLK_In	GDS83-88_CLK_Out	GDS83-88_CLK_In	GDS83-88_CLK_Out	GDS83-88_CLK_In	GDS83-88_CLK_Out
Standard GDS-Lines		GDS89-94_CLK_In	GDS89-94_CLK_Out	GDS89-94_CLK_In	GDS89-94_CLK_Out	GDS89-94_CLK_In	GDS89-94_CLK_Out
		GDS89-94_CLK_In	GDS89-94_CLK_Out	GDS89-94_CLK_In	GDS89-94_CLK_Out	GDS89-94_CLK_In	GDS89-94_CLK_Out
Standard GDS-Lines		GDS95-100_CLK_In	GDS95-100_CLK_Out	GDS95-100_CLK_In	GDS95-100_CLK_Out	GDS95-100_CLK_In	GDS95-100_CLK_Out
		GDS95-100_CLK_In	GDS95-100_CLK_Out	GDS95-100_CLK_In	GDS95-100_CLK_Out	GDS95-100_CLK_In	GDS95-100_CLK_Out
Standard GDS-Lines		GDS101-106_CLK_In	GDS101-106_CLK_Out	GDS101-106_CLK_In	GDS101-106_CLK_Out	GDS101-106_CLK_In	GDS101-106_CLK_Out
		GDS101-106_CLK_In	GDS101-106_CLK_Out	GDS101-106_CLK_In	GDS101-106_CLK_Out	GDS101-106_CLK_In	GDS101-106_CLK_Out

MGT	MGT connection (optional and defined by DESY Zone 3 connector pin assignment recommendation) The number of MGTs is dependent on the chosen interface class. Class D1.1 has 2 MGT links. CLK_OUT is an output of the AMC (driven by AMC) and usually derived from the MGT clock generator. CLK_IN is an output of the RTM (driven by RTM) that usually carries the MGT reference clock for direct connection to FPGA MGT bank (MGT_REFCLK). Clock IO standard is LVDS. MGT IO standard is CML. Modern DESY boards have AMC coupling capacitors on all MGT TX and RX lines. The CLK_OUT input (AMC to RTM) is usually DC-coupled on the AMC. The clock output (RTM to AMC) is usually AMC coupled on the FPGA (FPGA requirement for MGT reference clocks) TX means output of AMC (AMC to RTM). RX means input of AMC (RTM to AMC).
-----	--

RTM_IO	
RTM_00_CC_P	RTM_I000_CC_P
RTM_00_CN	RTM_I000_CN_N
RTM_01_P	RTM_I001_P
RTM_01_N	RTM_I001_N
RTM_02_P	RTM_I002_P
RTM_02_CN	RTM_I002_CN
RTM_03_CC_P	RTM_I003_CC_P
RTM_03_CN	RTM_I003_CN_N
RTM_04_P	RTM_I004_P
RTM_04_N	RTM_I004_N
RTM_05_P	RTM_I005_P
RTM_05_N	RTM_I005_N
RTM_06_P	RTM_I006_P
RTM_06_N	RTM_I006_N
RTM_07_P	RTM_I007_P
RTM_07_N	RTM_I007_N
RTM_08_CC_P	RTM_I008_CC_P
RTM_08_CN	RTM_I008_CN_N
RTM_09_P	RTM_I009_P
RTM_09_N	RTM_I009_N
RTM_10_P	RTM_I010_P
RTM_10_N	RTM_I010_N
RTM_11_CC_P	RTM_I011_CC_P
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RTM_14_P	RTM_I014_P
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RTM_20_N	RTM_I020_N
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RTM_21_N	RTM_I021_N
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RTM_23_N	RTM_I023_N
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RTM_24_CN	RTM_I024_CN_N
RTM_25_P	RTM_I025_P
RTM_25_N	RTM_I025_N
RTM_26_P	RTM_I026_P
RTM_26_N	RTM_I026_N
RTM_27_CC_P	RTM_I027_CC_P
RTM_27_CN	RTM_I027_CN_N
RTM_28_P	RTM_I028_P
RTM_28_N	RTM_I028_N
RTM_29_P	RTM_I029_P
RTM_29_N	RTM_I029_N
RTM_30_P	RTM_I030_P
RTM_30_N	RTM_I030_N
RTM_31_P	RTM_I031_P
RTM_31_N	RTM_I031_N
RTM_32_CC_P	RTM_I032_CC_P
RTM_32_CN	RTM_I032_CN_N
RTM_33_P	RTM_I033_P
RTM_33_N	RTM_I033_N
RTM_34_P	RTM_I034_P
RTM_34_N	RTM_I034_N
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RTM_35_CN	RTM_I035_CN_N
RTM_36_P	RTM_I036_P
RTM_36_N	RTM_I036_CN_N
RTM_37_P	RTM_I037_P
RTM_37_N	RTM_I037_N
RTM_38_P	RTM_I038_P
RTM_38_N	RTM_I038_N
RTM_39_CC_P	RTM_I039_CC_P
RTM_39_CN	RTM_I039_CN_N
RTM_40_P	RTM_I040_P
RTM_40_N	RTM_I040_N
RTM_41_P	RTM_I041_P
RTM_41_N	RTM_I041_N

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FILENAME: RTM_Zone3.SchDoc

Project Title:
RTM-Template.PrjPcb
Schematic Title:
Zone 3 Connector
DATE: 06.02.2024

Engineer 1:	Robert Wedel
Engineer 2:	Michael Fenne



Rev: 0.7
Size: A3
Sheet:

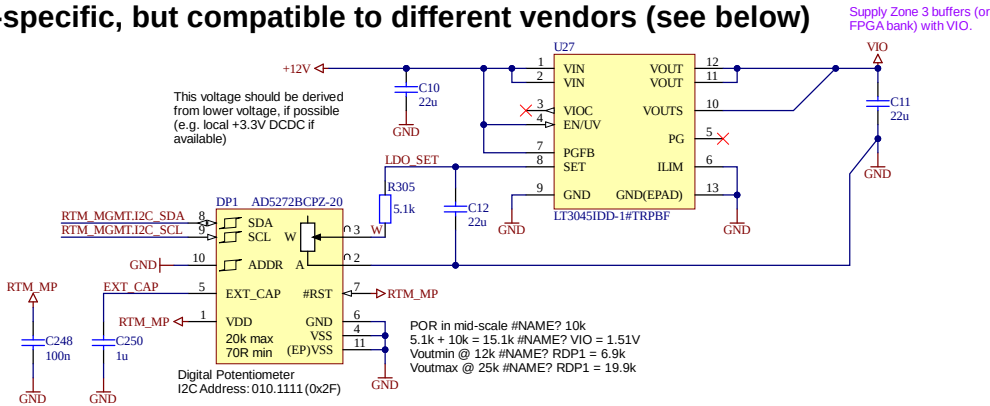
Single-Ended IOs (optional)

LVDS only - no single ended IOs (recommended)

No extra components needed, ignore this page!

DESYS recommends to use only LVDS signals on all RTM-IO pins. LVDS is a common standard and will always be compatible, independent of FPGA bank IO voltage. By using LVDS signals only, no glue logic, no voltage translation and no coupling capacitors are necessary. Translating single-ended interfaces (such as SPI) to LVDS to cross Zone 3 is preferred and requires no variable voltage supply or interaction with MMC management. However, there are cases (e.g. where more signals need to be transferred over Zone 3 than pins are available) where the user decides to use single-ended IOs. In this case, a variable IO voltage on all these signals is needed. Depending which FPGA type and which bank voltage was chosen on the AMC, the voltage of the Zone 3 has to be configured to precisely match the FPGA bank voltage. Failing to adhere to the specific bank voltage requirement will exceed the absolute maximum ratings, may damage the AMC and will not work, in any case. A circuit for the bank voltage setting is highly proprietary and has to be specifically supported by the module management controller (MMC) on the AMC. The following implementations are supported by DESYS MMC. Single-ended RTM IOs shall be avoided wherever possible.

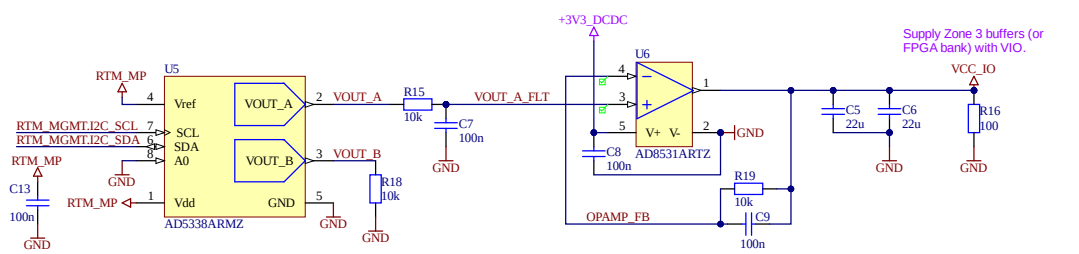
Single-ended IO voltage generation with LDO
DESYS-specific, but compatible to different vendors (see below)



Depending on the chosen FPGA bank voltage on AMC, a matching Zone 3 voltage has to be selected. Old FPGAs (Virtex®-4, Virtex®-5 support bank voltages of up to 3.3V. Most DESYS boards used 2.5V bank voltage on the Zone3 interface. Modern FPGAs (Ultrascale® and newer) mostly support 1.8V on Zone 3 only. If single-ended IOs on Zone 3 are needed, DESYS recommends this circuit. The MMC on the AMC will set up the digital potentiometer in such a way that LDO generates the IO voltage that matches the specific FPGA bank voltage. It is supported by DESYS MMC Stamp and support will be added to the MMC of older DESYS designs such as DAMC-FMC25, DAMC-FMC20 and DAMC-TCK7.

The digital potentiometer can be programmed to a fixed start-up value (non-volatile memory). Support of one specific 3rd-party AMC board can be achieved by programming a fixed value into the resistor, resulting in a correct (but fixed) Zone 3 voltage. If the AMC board is changed, the potentiometer may have to be re-programmed with a different value. This solution is, even if it is proprietary, the most flexible way to allow single-ended IO compatibility across multiple vendors and MMC solutions, respectively.

Single-Ended IO voltage generation with DAC (legacy, not recommended)



This is the solution is used on all legacy DESYS RTMs (DRTM-AD84, DRTM-PZT4, DRTM-DWC10, DRTM-DWC8VM1, etc.). It is also supported by Struck SIS8300L2 and SIS8325 and SIS8300KU. This concept uses a DAC that is controlled by the MMC on the AMC. The disadvantage of the solution is that it only supports currents up to 250mA, it needs external voltage (+3V3_DCDC here) and the AMC has to be aware of this solution and has to specifically support it. 3rd-party AMCs that are not adapted to this solution, can not operate the RTM at all. However, all existing AMCs with DESYS MMC V1.00 or DESYS MMC Stamp will support this solution out-of-the-box.



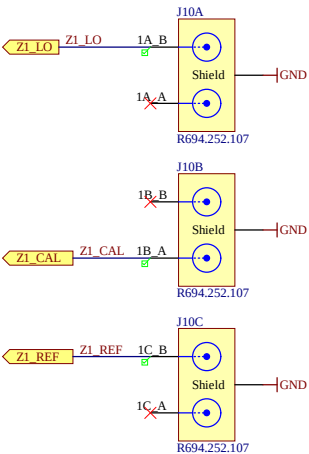
 Notkestrasse 85 22607 Hamburg mtca-techlab@desy.de	Project Title: RTM-Template.PrjPcb Schematic Title: Zone 3 single-ended IO DATE: 06.02.2024 20:14:59			
	DESYS reserves all rights according to ISO 16016. © 2024		Engineer 1: Michael Fenner Engineer 2: Johannes Zink	Rev: 0.7 Size: A3 Sheet: 3 of 4
	FILENAME: RTM_Single_Ended_IO.SchDoc			

RTM Backplane Connectors (optional)

The MicroTCA specification Revision 4.1 defines an optional RTM backplane. It is used for distribution of high-precision clocks inside the chassis to MicroTCA RTMs. In addition, a clean bipolar supply voltage can be distributed on this backplane. Special eRTMs (without connection to AMC backplane) generate precision clocks and reference signals for the RTMs. A special rear power module can generate a clean supply voltage for the RTMs. Management of the eRTMs and rear power supplies is realised by using a MCH-RTM, which forwards the rear management signals the front MCH.

A 12-slot chassis with the shown RTM backplane is available from nVent / Schroff GmbH. A modular rear power module and the MCH-RTM are available from N.A.T. GmbH. The DRTM-LOG1300 is available from DESY.

RTM Backplane Zone 1
RF cock input



connector pinout for slots #4-#12

	A	B
1A	rfu	LO
1B	CAL	rfu
1C	rfu	REF

rfu – pins reserved for future use

RF_CONF Settings

The voltage on RF_CONF is used to request a specific clock assignment on the Zone1 and Zone 2 connectors. A fixed voltage coming from a simple resistor divider can be presented here. Alternatively the voltage can be generated using an electronic potentiometer for maximum flexibility. (5V supply is required for full scale setting.)

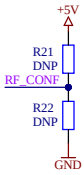
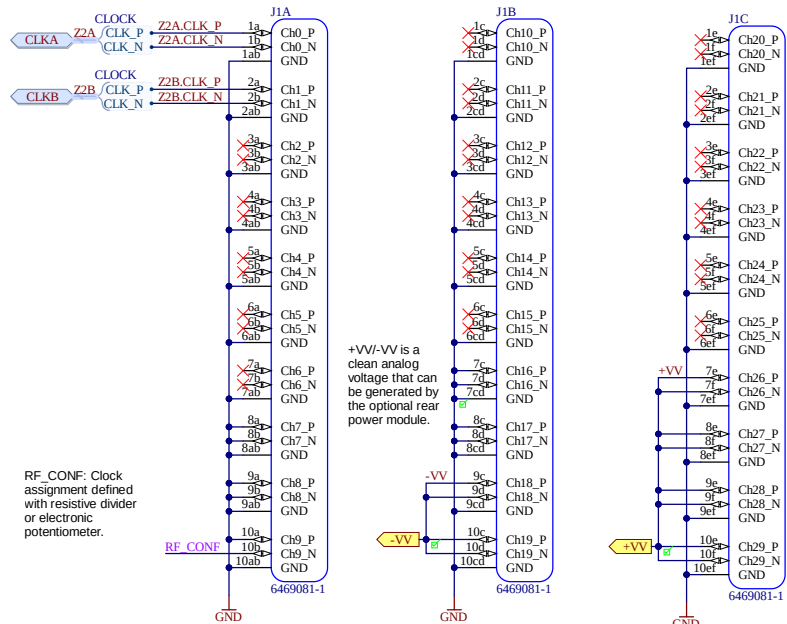


Table 3: RF_CONF signal voltage levels and their assignment

State	CLKs LO CAL REF [1=yes, 0=no]	Required DC level [V]	Lower limit [V]	Upper limit [V]
1	0000	0.4	0.26	0.54
2	0001	0.68	0.54	0.82
3	0010	0.96	0.82	1.1
4	0011	1.24	1.1	1.38
5	0100	1.52	1.38	1.66
6	0101	1.8	1.66	1.94
7	0110	2.08	1.94	2.22
8	0111	2.36	2.22	2.5
9	1000	2.64	2.5	2.78
10	1001	2.92	2.78	3.06
11	1010	3.2	3.06	3.34
12	1011	3.48	3.34	3.62
13	1100	3.76	3.62	3.9
14	1101	4.04	3.9	4.18
15	1110	4.32	4.18	4.46
16	1111	4.6	4.46	4.74

RTM Backplane Zone 2
Analog voltage and additional clocks



+VV/-VV is a clean analog voltage that can be generated by the optional rear power module.

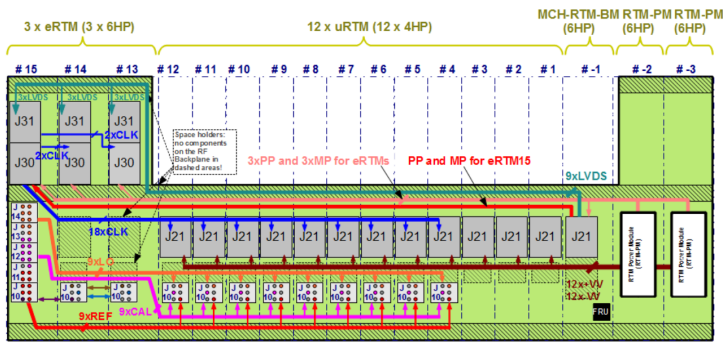
RF_CONF: Clock assignment defined with resistive divider or electronic potentiometer.

Table 20: J21 connector pinout for slots #4-#12

	a	b	ab	c	d	cd	e	f	ef
1	CLKxA_P	CLKxA_N	GND	rfu	rfu	GND	rfu	rfu	GND
2	CLKxB_P	CLKxB_N	GND	rfu	rfu	GND	rfu	rfu	GND
3	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
4	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
5	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
6	rfu	rfu	GND	rfu	rfu	GND	rfu	rfu	GND
7	rfu	rfu	GND	GND	GND	GND	+VV	+VV	GND
8	GND	GND	GND	GND	GND	GND	+VV	+VV	GND
9	GND	GND	GND	-VV	-VV	GND	+VV	+VV	GND
10	PS1#	RF_CONF	GND	-VV	-VV	GND	+VV	+VV	GND

rfu – pins reserved for future use

Connectivity of DESY RTM Backplane



DRTM-LOG1300 - eRTM clock generator



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Project Title:
RTM-Template.PrjPcb
Schematic Title:
RTM Backplane Connectors
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Engineer 1: Michael Fenner
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Rev: 0.7
Size: A3
Sheet:
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FILENAME: RTM_Backplane.SchDoc